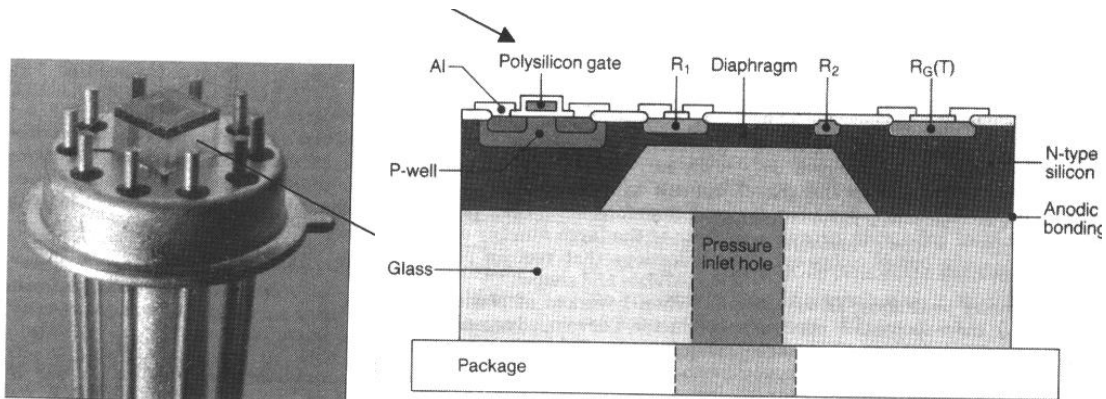


Lecture 11 MEMS Packaging

◆ The Needs for MEMS packaging

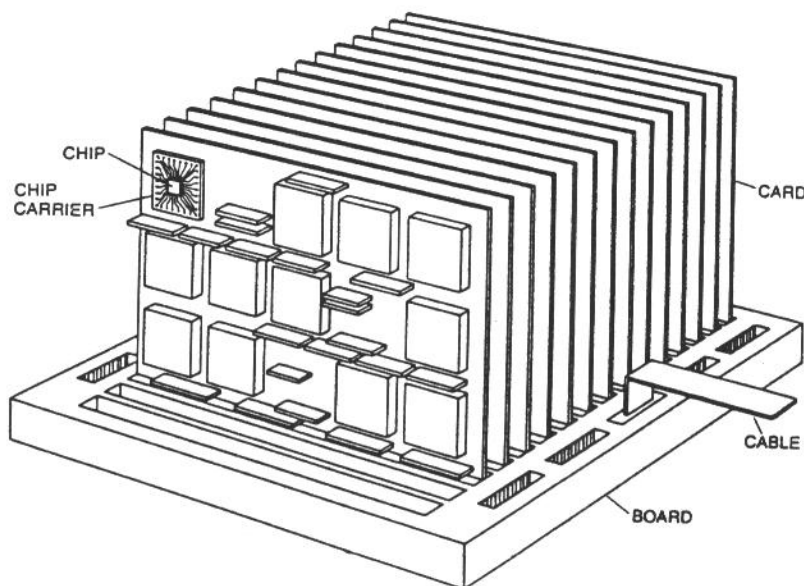


Package of a pressure sensor

1. **Signal redistribution** – fans out signal lines to larger/easier management surface (similar to ICs)
2. **mechanical support** – rigidity, stress release, protection from environment (similar to ICs)
3. **power distribution** – provides power (similar to ICs)
4. **thermal management** – to sustain device on operation condition (similar to ICs)
5. **Fluid management** – provides fluids
6. **Part of the device** – for example: sensors (pressure, accelerometer...), flow management systems (μ pump, flow channel, μ valve...)
7. **Sealing need for higher performance or material storage/preservation** – high Q need (high vacuum sealing for resonant device, enhanced from 100 to 10,000), stable operation environment (inner gas sealing for optical switch, μ lamp), liquid sealing need (liquid actuator, biomedical reagent/chemical storage/preservation, fuel/combustion material storage)...., etc.

8. Assembly need – for example: device batch transfer, parts self-assembly

◆ Different Levels of MEMS packaging (analog to IC packaging)



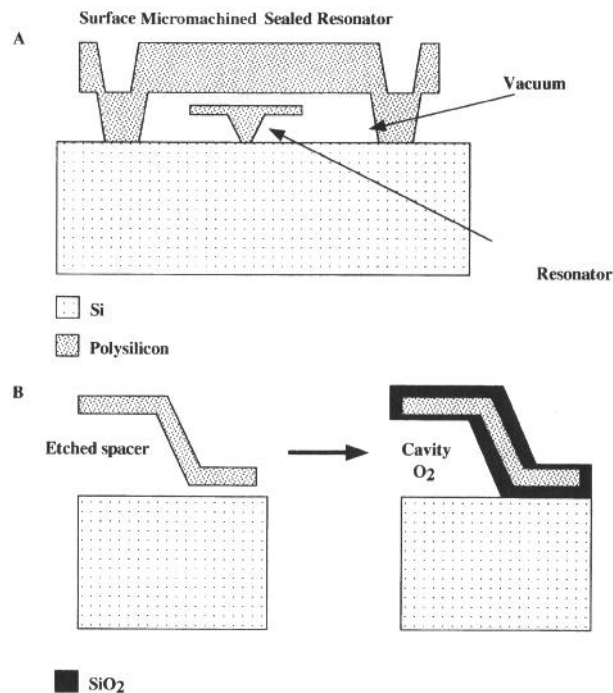
IC packaging hierarchy

1. L_0 level packaging: encapsulating a die features on wafer (component level)
2. L_1 level packaging: packaging a whole die at a time (die level)
3. L_2 level packaging: packaging between dies (circuit board level)
4. L_3 level packaging: packaging between circuit board (chassis or box level)
5. L_4 level packaging: packaging between chassis/box (system level)
6. L_5 level packaging: packaging between Systems

◆ Thin Film Deposition/Growth Bonding (L_0 and L_1)

1. Reactive sealing

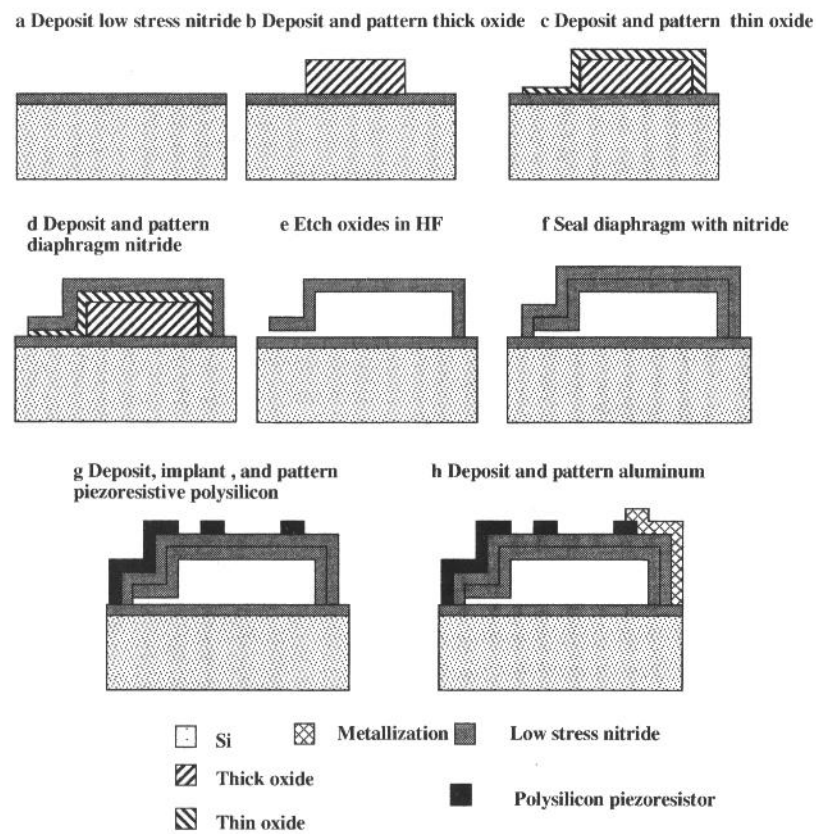
- ▲ Thermal oxidation silicon and poly-silicon at 1000°C
- ▲ Oxygen is reacted away inside cavity to create vacuum
- ▲ Require a long etching process to remove sacrificial layer inside cavity.



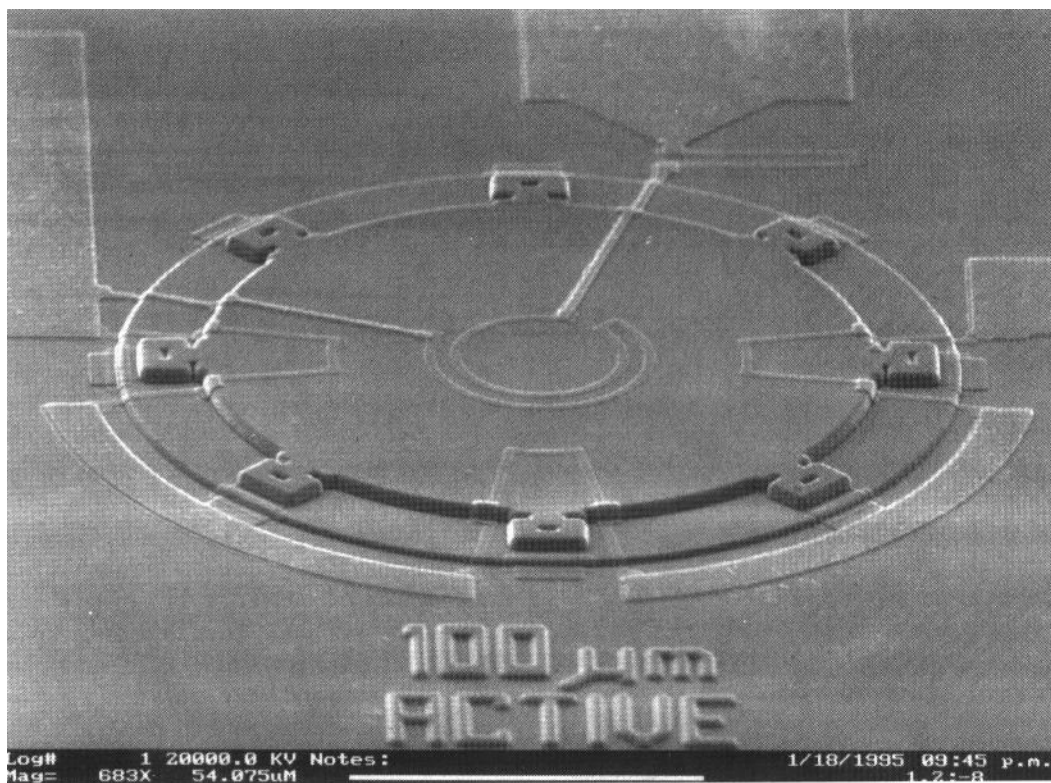
Reactive sealing

2. Sealant film sealing

- ▲ LPCVD silicon oxide (450°C, 200-300 mTorr) and silicon nitride (850°C, 200-300 mTorr) or PECVD oxide or nitride (250-350 °C, 200-300 mTorr)
- ▲ Thinner film required for higher temp films. (need 0.1-1μm sealant materials for 0.2 μm thick etching hole sealing)
- ▲ Create vacuum about 67 to 300 mTorr
- ▲ Cavity pressure is stable, but variable across a substrate and from wafer to wafer
- ▲ Require a long etching process to remove sacrificial layer inside cavity.



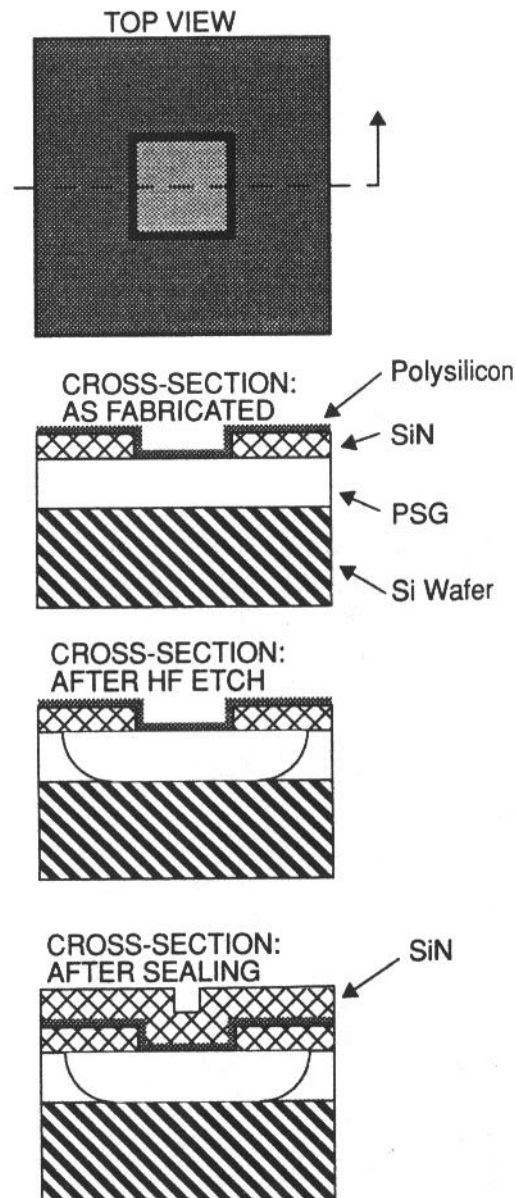
Sealant film sealing



Sealed absolute pressure sensor

3. Permeable polysilicon sealing

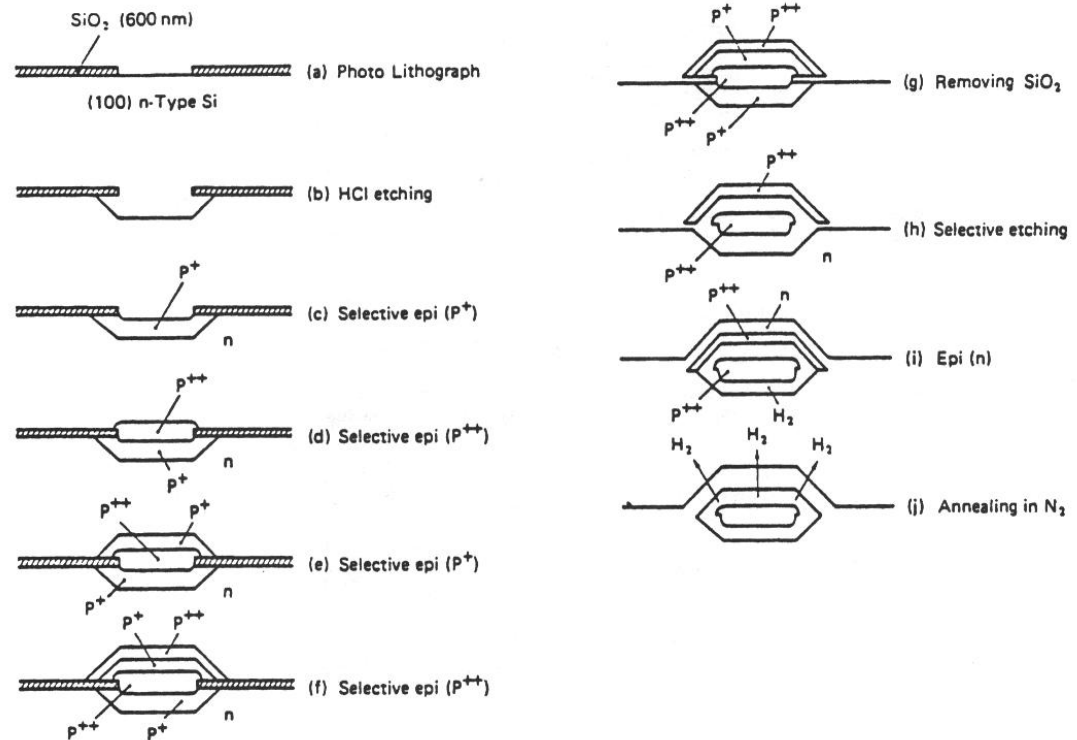
- ▲ Use permeable polysilicon as etching windows (etchant goes through the grain boundary)
- ▲ $3\mu\text{m}$ deep and 1mm wide cavity can be etched in 120 second.
- ▲ Use only 10 nm low-stress silicon nitride for hermetic sealing.



Permeable polysilicon sealing

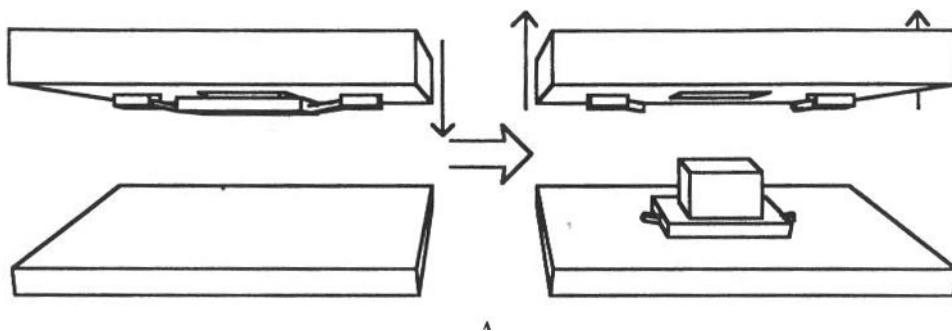
4. Epitaxial Si sealing

- ▲ Require silicon substrate for expi
- ▲ Tedious and expensive

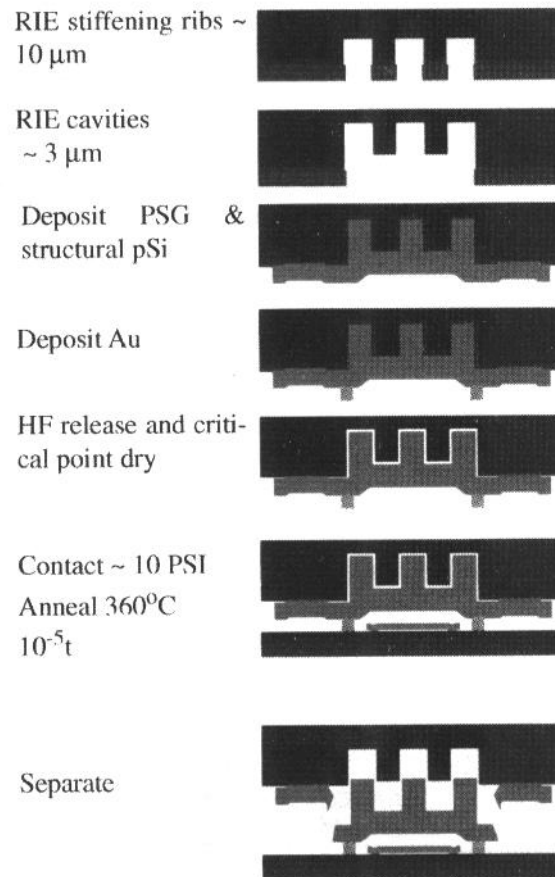


5. Low temp wafer transfer

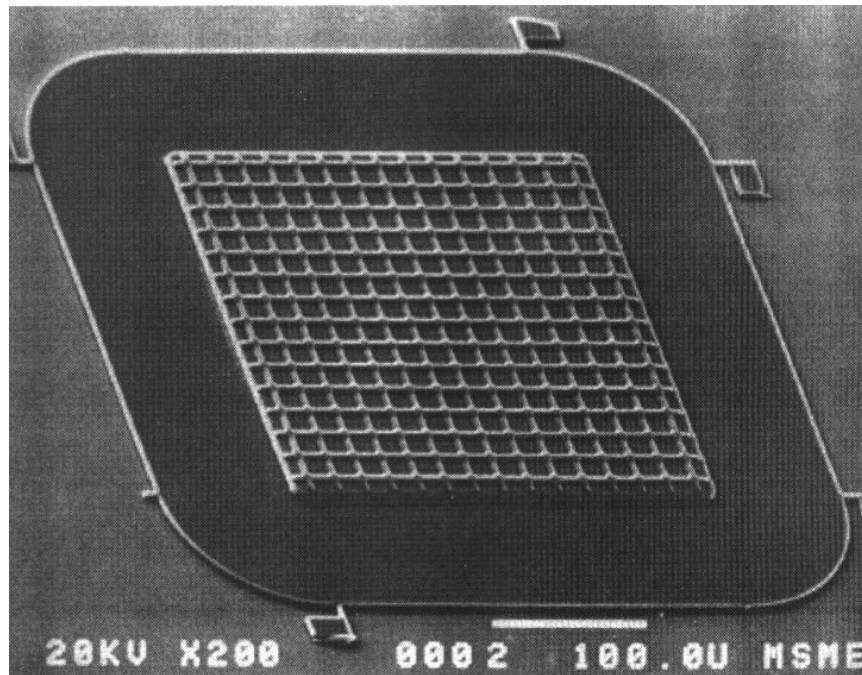
- ▲ Use low temp (363°) Au-Si eutectic bonding



Wafer to wafer transfer of encapsulation structures



HEXSIL process

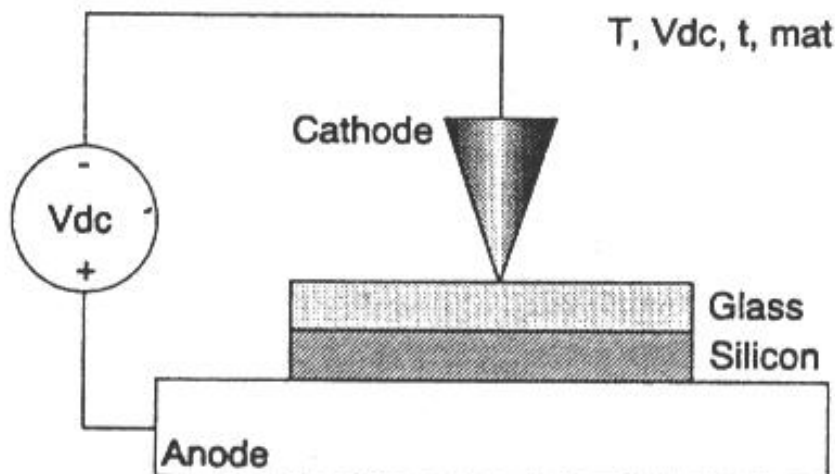


SEM picture of a transferred cap

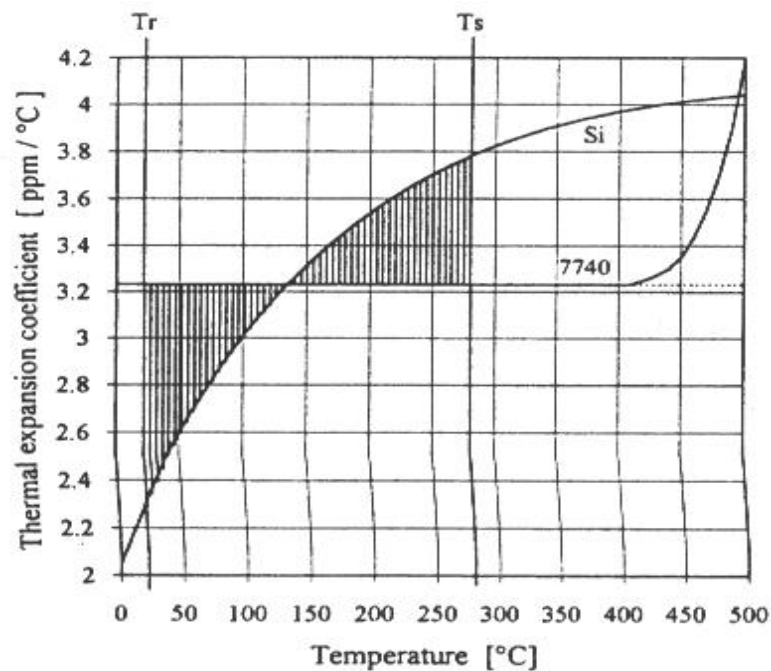
◆ **Thermal Bonding (L_0 or L_1)**

1. Field-assisted thermal bonding (Anodic bonding, Electrostatic bonding, Mallory process)

- ▲ Bonding metals to sodium-rich glass (for example: Corning #7740 (Pyrex), #7070, soda lime #0080, potash soda lead #0120, and aluminosilicate #1720)
- ▲ Pyrex is most suitable for Si-Glass bonding.
- ▲ Negative voltage connected to heated glass to attract positive ion inside glass while Si connected to ground. Strong electrical field built in Si-glass interface.
- ▲ Temp required 180-500°C, Voltage: 200-1000V, time required: 5-60 min.
- ▲ Surface roughness need: $R_a < 1 \mu\text{m}$
- ▲ Native/thermal oxide on Si < 200 nm
- ▲ For pyrex bonding, silicon under tension is preferred, in which bonding temp is beyond 280°C in theory (315°C by experiment)



Anodic bonding



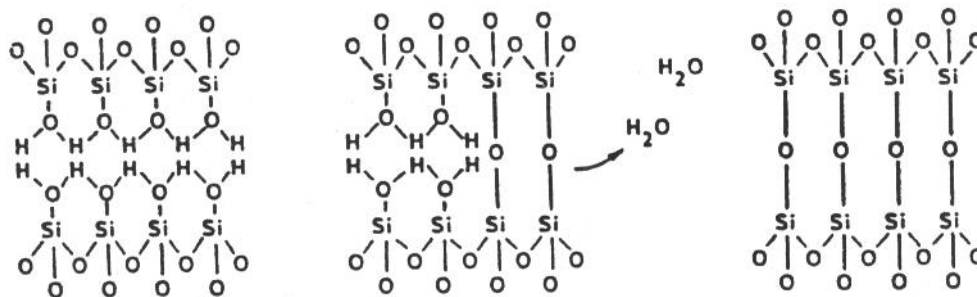
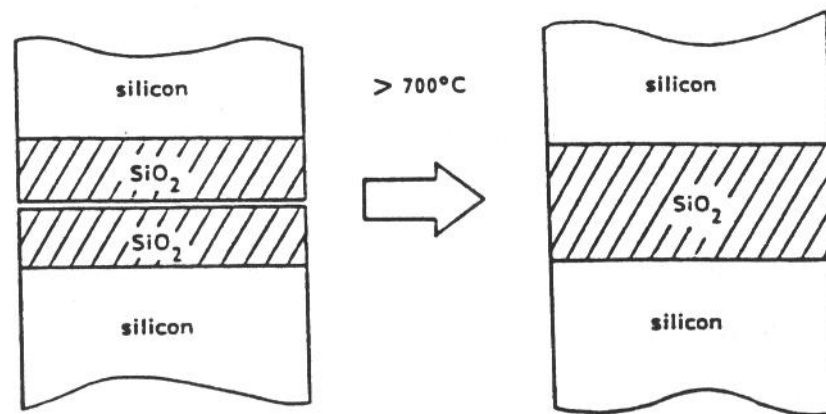
Thermal expansion Coefficient of Si and Pyrex

2. Modifications of field-assisted thermal bonding

- ▲ **Ti mesh bias electrode to reduce bonding voltage**
- ▲ **Bond glass on Al/SiO₂/Si or Polysilicon/SiO₂/Si to protect Si from high electrical field**
- ▲ **Two silicon wafers with thin (4-7 μm) sputtered pyrex on thermal SiO₂/Si substrate, with low voltage of 30-60V and 450-550°C**
- ▲ **Bonding of a bare Si wafer to a second wafer with oxide failed for oxide breakdown under small applied bias.**

3. Thermal silicon fusion bonding

- ▲ **High temp (> 800°C) and oxidizing environment.**
- ▲ **Bonding strength ~20 MPa**
- ▲ **Surface roughness: <4 nm**
- ▲ **Small pressure during bonding can increase bonding strength**
- ▲ **Bonding can be done on bare Si to bare Si, oxidized Si and bare Si, and two oxidized Si. Nitride can replace oxide for bonding. (thickness around 100-200 nm)**
- ▲ **Hydration is desired before fusion bonding. Wafer treated with H₂O₂-H₂SO₄, dilute H₂SO₄, or boiling HNO₃**



Thermal silicon fusion bonding

4. Thermal thin glass film bonding

- ▲ LPCVD PSG (phosphosilicate glass) between Si wafer: need 1100 °C, 30 mins.
- ▲ Glass frits (Corning #75xx) with sealing temp 415-650°C and slight pressure (>1 psi) by screen-printing, spraying
- ▲ APCVD boron oxide at 450°C
- ▲ Spin-on-glass (SOG) at 250°C and pressurized under vacuum environment for 1 hr, then annealed at 1150°C

5. Eutectic bonding

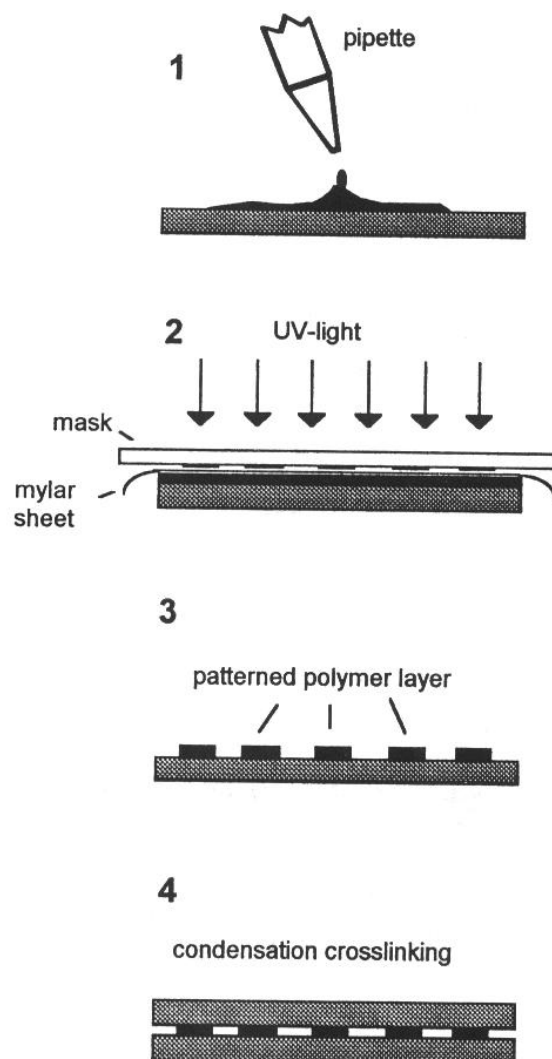
- ▲ Au-Ti eutectic bonding at 363°C, with strength of 148 MPa possible
- ▲ Hard to get complete bonding over large areas
- ▲ Native oxide to prevent bonding
- ▲ Long term drift due to relaxation for built in stress
- ▲ Bonding strength ~148 Mpa.

◆ **Chemical Reaction Bonding (L_1)**

- ▲ Use dilute HF (1%) with pressure (1.6MPa) to bond Si/Si, SiO₂/Si and SiO₂/ SiO₂ substrate.

◆ **Organic intermediate material bonding (L_0 and L_1)**

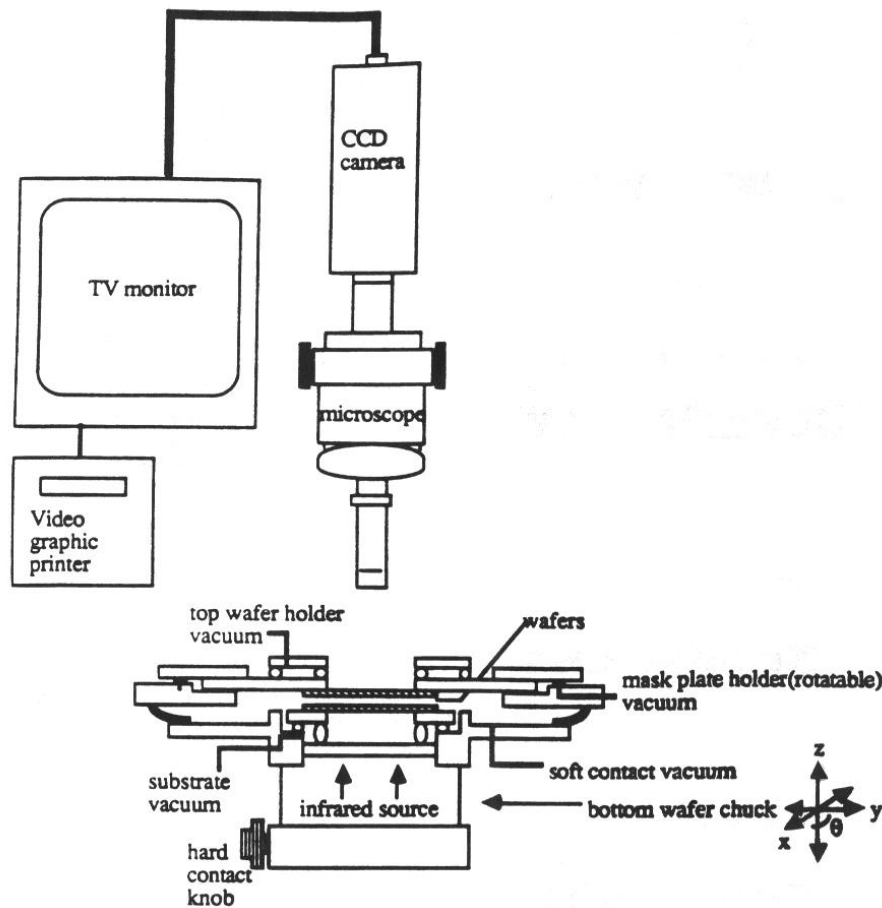
- ▲ Use thick PR, polyimides, AZ-4000, SU-8, PMMA, PLG, adhesive, UV curable resins.
- ▲ Low bonding temp, bond strength can be high, no metal ions are present, elastic properties can release stress
- ▲ Impossibility of hermetic seal, high vapor pressure, poor mechanical properties.



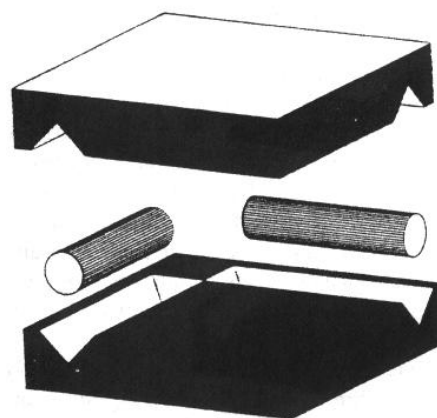
Silicon/polymer/silicon bonding

◆ **Alignment during packaging**

- ▲ **Hole generation on both wafers: 50 μm accuracy**
- ▲ **Bonding machine: 2.5 μm**
- ▲ **Optical fiber assisted alignment: 5 μm (no need of microscope)**



Bonding machine



Optical fiber assisted alignment

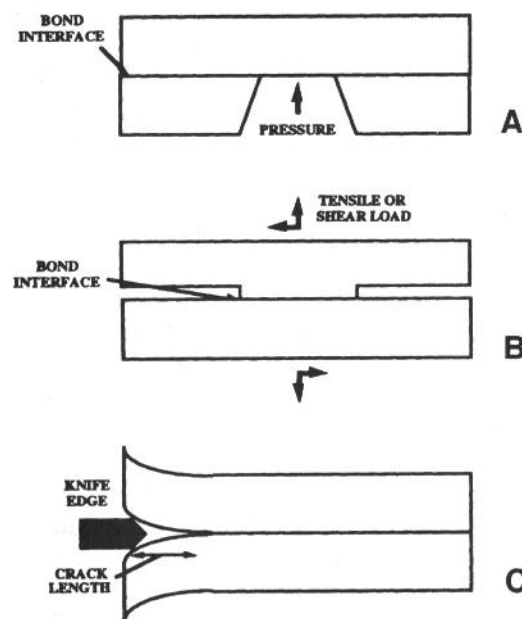
◆ **Testing of packaging quality**

1. bonding voids investigation

- ▲ infrared transmission (20-30 μm voids)
- ▲ ultrasonic (qualitative)
- ▲ X-ray topography

2. Bonding strength investigation

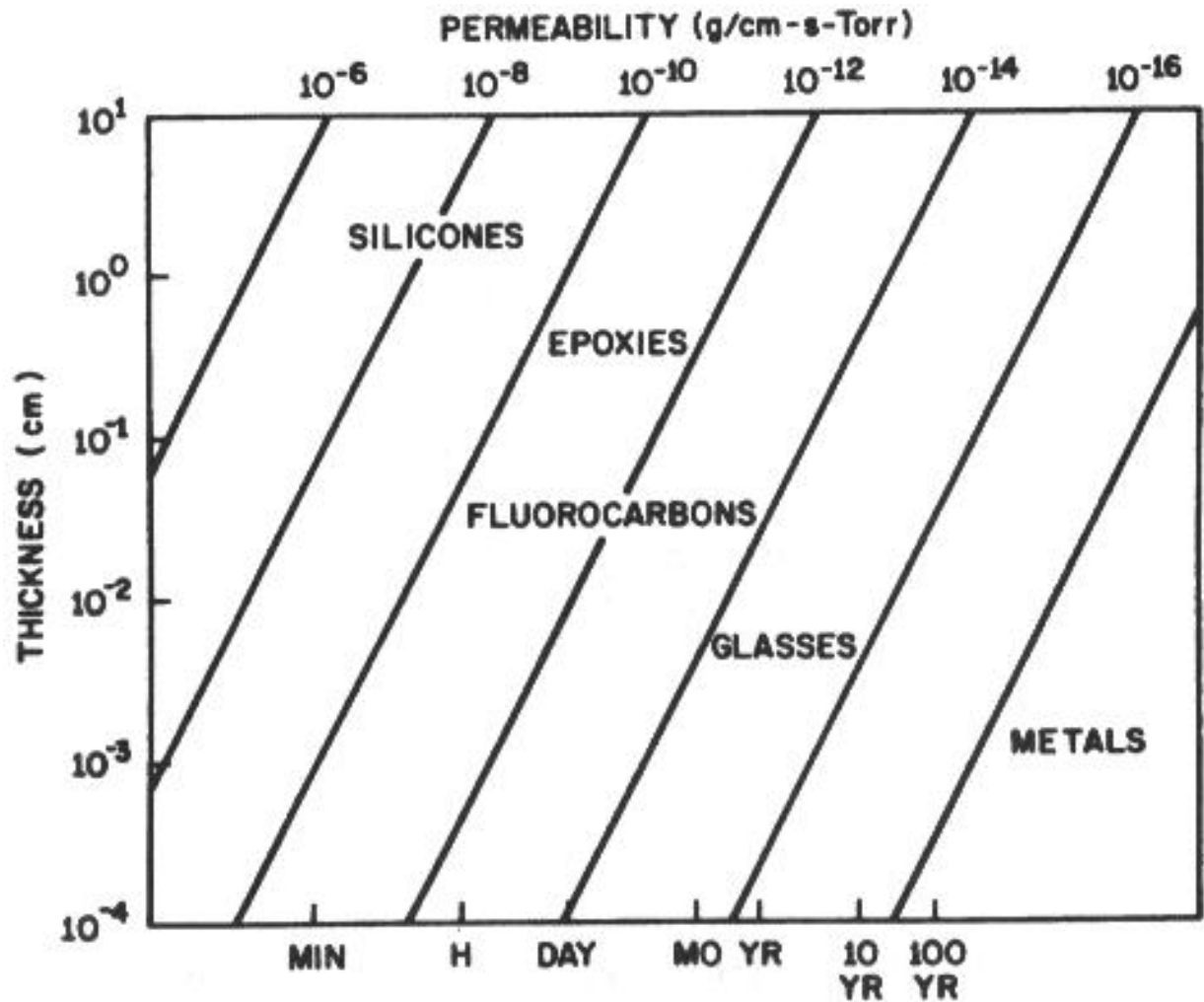
- ▲ Burst test (A)
- ▲ Tensile and shear test (B)
- ▲ Maszera test (C)



Bonding strength testing

3. Hermetic sealing testing

- ▲ Dynamic helium leak detection (5×10^{-11} to 5×10^{-10} Torr/sec)
- ▲ Measuring gas concentration inside sealed cavity
Fourier (FTIR), using N_2O as tracer gas
- ▲ Measure the deflection of a thin membrane covering the cavity



The calculated time for moisture to permeate various sealant materials (50% of the exterior humidity)

Reference:

Fundamentals of Microfabrication, Marc Madou, CRC press, pp. 378-395, 1997