Lecture 3-2 IC Fabrication Process-II: Diffusion, Ion implantation, Film deposition, Interconnection and contacts

- **Diffusion process:**
  The deposition of high concentration of the desired impurity on the silicon surface through windows, and then move the impurity atoms from the surface into the silicon crystal.

1. Substitutional diffusion and interstitial diffusion

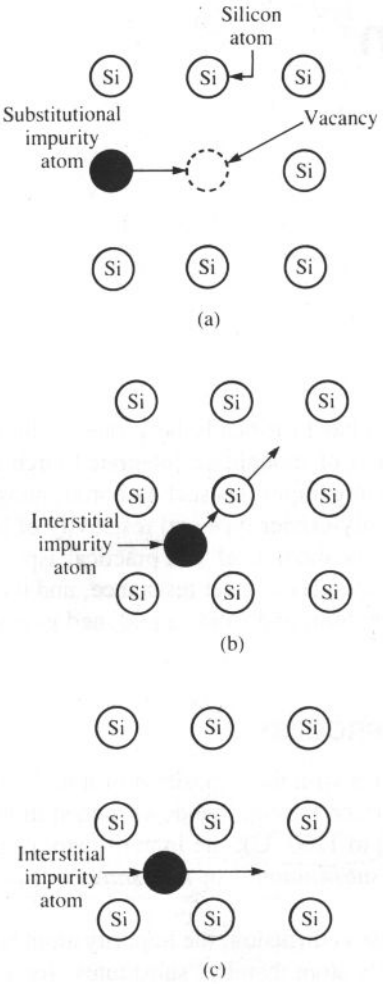


Fig. 4.1 Atomic diffusion in a two-dimensional lattice. (a) Substitutional diffusion, in which the impurity moves among vacancies in the lattice; (b) interstitialcy mechanism, in which the impurity atom replaces a silicon atom in the lattice, and the silicon atom is displaced to an interstitial site; (c) interstitial diffusion, in which impurity atoms do not replace atoms in the crystal lattice.

2. Mathematical Model for diffusion:

Fick's first law of diffusion:

$$J = -D\frac{\partial N}{\partial x} \tag{3-1}$$

J: Particle flux of the donor or acceptor impurity species, N: concentration of the impurity, D: Diffusion coefficient.

Continuity equation:

$$\frac{\partial N}{\partial t} = -\frac{\partial J}{\partial x} \tag{3-2}$$

Combine (3-1) and (3-2) yields *Fick's second law of diffusion:*

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2} \tag{3-3}$$

Assumption: D is independent of position.

2.1 Constant source diffusion:

$$N(x,t) = N_0 erfc(\frac{x}{2\sqrt{Dt}}) \tag{3-4}$$

N_0: the impurity concentration at the wafer surface

The dose Q (atoms/cm^2):

$$Q = \int_0^\infty N(x,t)dx = 2N_0\sqrt{Dt/\pi} \tag{3-5}$$

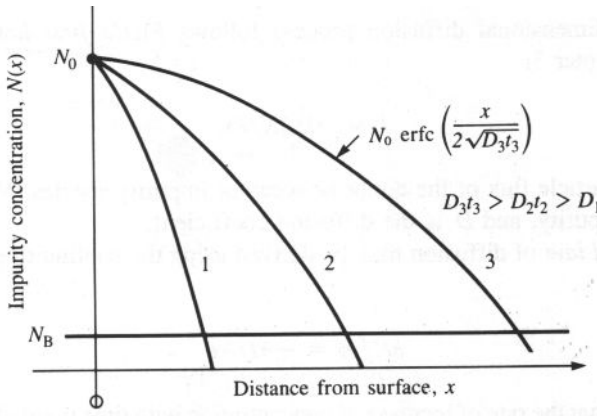


Fig. 4.2 A constant-source diffusion results in a complementary error function impurity distribution. The surface concentration N_0 remains constant and the diffusion moves deeper into the silicon wafer as the Dt product increases. Dt can change as a result of increasing diffusion time, increasing diffusion temperature, or a combination of both.

2.2Limited source diffusion:

$$N(x,t) = (Q/\sqrt{\pi Dt})\exp^{-(x/2\sqrt{Dt})^2} \qquad (3\text{-}6)$$

⇨ Gaussian distribution

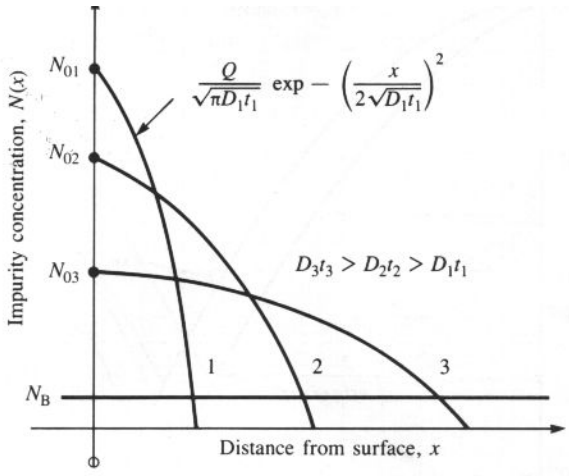


Fig. 4.3 A Gaussian distribution results from a limited-source diffusion. As the Dt product increases, the diffusion front moves more deeply into the wafer and the surface concentration decreases. The area under each of the three curves is the same.

2.3 Two-step diffusion:

A short constant-source diffusion is often followed by a limited-source diffusion. The constant-source diffusion step is used to, establish a known dose in a shallow layer (**predeposition step**), then the second limited diffusion step (**drive-in step**) move the diffusion front to the desire depth.

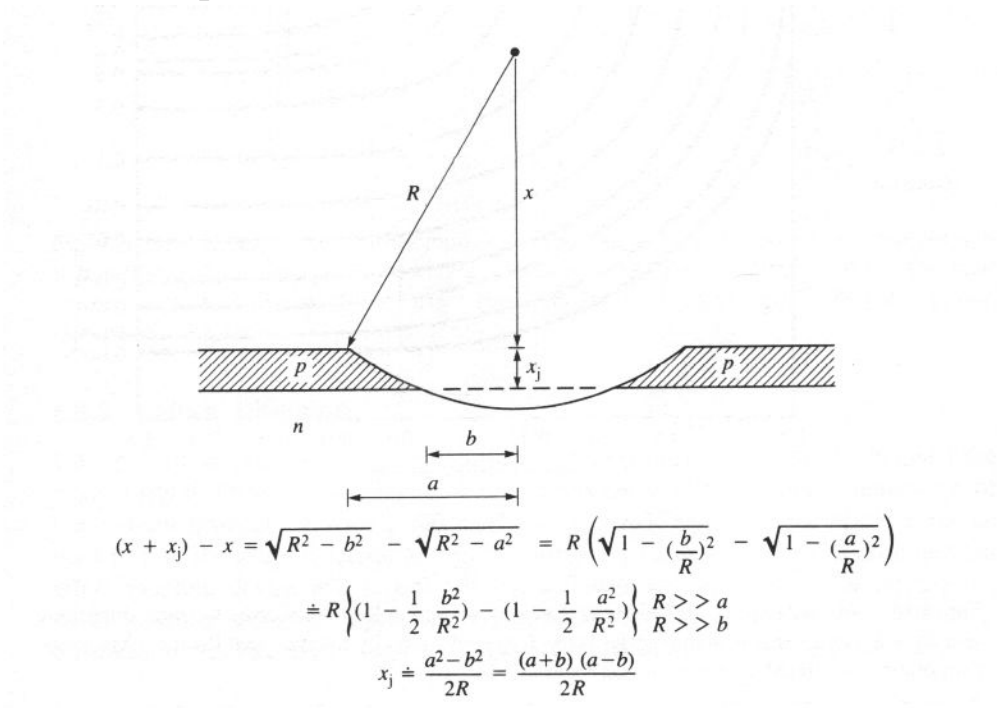
If Dt product of the predeposition step much greater: erfc function distribution

If Dt product of the drive-in step much greater: Gaussian function distribution

2.4 Successive diffusion:

$$(Dt)_{tot} = \sum_i D_i t_i \tag{3-7}$$

3. Junction-Depth Measurement:



$$(x + x_j) - x = \sqrt{R^2 - b^2} - \sqrt{R^2 - a^2} = R\left(\sqrt{1 - (\frac{b}{R})^2} - \sqrt{1 - (\frac{a}{R})^2}\right)$$

$$\doteq R\left\{(1 - \frac{1}{2}\frac{b^2}{R^2}) - (1 - \frac{1}{2}\frac{a^2}{R^2})\right\} \begin{matrix} R >> a \\ R >> b \end{matrix}$$

$$x_j \doteq \frac{a^2 - b^2}{2R} = \frac{(a+b)(a-b)}{2R}$$

Fig. 4.11 Junction-depth measurement by the groove-and-stain technique. The distances a and b are measured through a microscope, and the junction depth is calculated using eq. (4.11).

4. Sheet Resistance

$$R = (\frac{\rho}{t})(\frac{L}{W}) = R_s(\frac{L}{W}) \tag{3-8}$$

R: resistance, ρ :resistivity, L: length, W: width, t: thickness, R_s: sheet resistance.

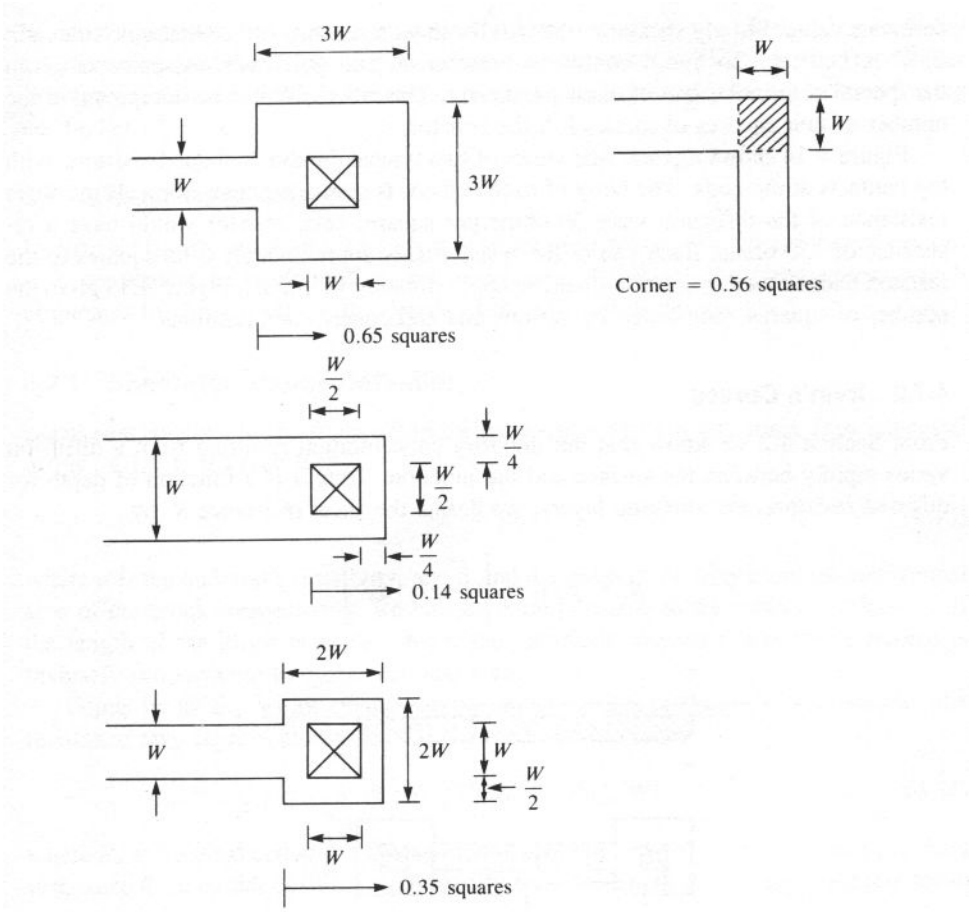


Fig. 4.15 Effective square contributions of various resistor end and corner configurations.

5. The Four–Point Probe:

$$\rho = 2\pi s V / I$$ ohm-meters for t >> s

$$\rho = (\pi t / \ln 2) V / I$$ ohm-meters for s >> t

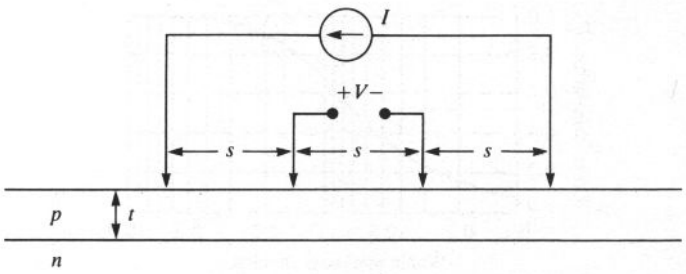


Fig. 4.17 Four-point probe with probe spacing s used for direct measurement of bulk wafer resistivity and the sheet resistance of thin diffused layers. A known current is forced through the outer probes, and the voltage developed is measured across the inner probes. (See eqs. (4.16) through (4.18).)

6. Diffusion System:

6.1 Boron diffusion:

· **Surface concentration can be: $4\times10^{20}/cm^3$**

· **Use boron trioxide (B_2O_3) to introduce boron—hard to strip=>use short oxidation step to help strip**

· $2B_2O_3 + 3Si \Leftrightarrow 4B + 3SiO_2$

· **Solid source: Trimethylborate (TMB), or Boron Nitride**

$$2(CH_3O)_3B + 9O_2 \xrightarrow{900°C} B_2O_3 + 6CO_2 + 9H_2O$$

· **Liquid source: boron tribromide (BBr_3)**

$$4BBr_3 + 3O_2 \rightarrow 2B_2O_3 + 6Br_2$$

· **Gaseous source: diborane (B_2H_6), poisonous and explosive, diluted with 99.9% Ar or N_2**

$$B_2H_6 + 3O_2 \xrightarrow{300°C} B_2O_3 + 3H_2O$$

and

$$B_2H_6 + 6CO_2 \xrightarrow{300°C} B_2O_3 + 6CO + 3H_2O$$

6.2 Phosphorus diffusion:

· **Surface concentration can be: $10^{21}/cm^3$**

· **Use phosphorus pentoxide (P_2O_5) to introduce phosphorus**

$$2P_2O_5 + 5Si \Leftrightarrow 4P + 5SiO_2$$

· **Solid source: ammonium monophosphate $NH_4H_2PO_4$ and ammonium diphosphate $(NH_4)_2H_2PO_4$**

· **Liquid source: phosphorus oxychloride ($POCl_3$)**

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2$$

· **Gaseous source: Phosphine (PH_3), poisonous and explosive, diluted with 99.9% Ar or N_2**

$$PH_3 + 4O_2 \longrightarrow P_2O_5 + 3H_2O$$

6.3 Open-furnace-tube diffusion systems:

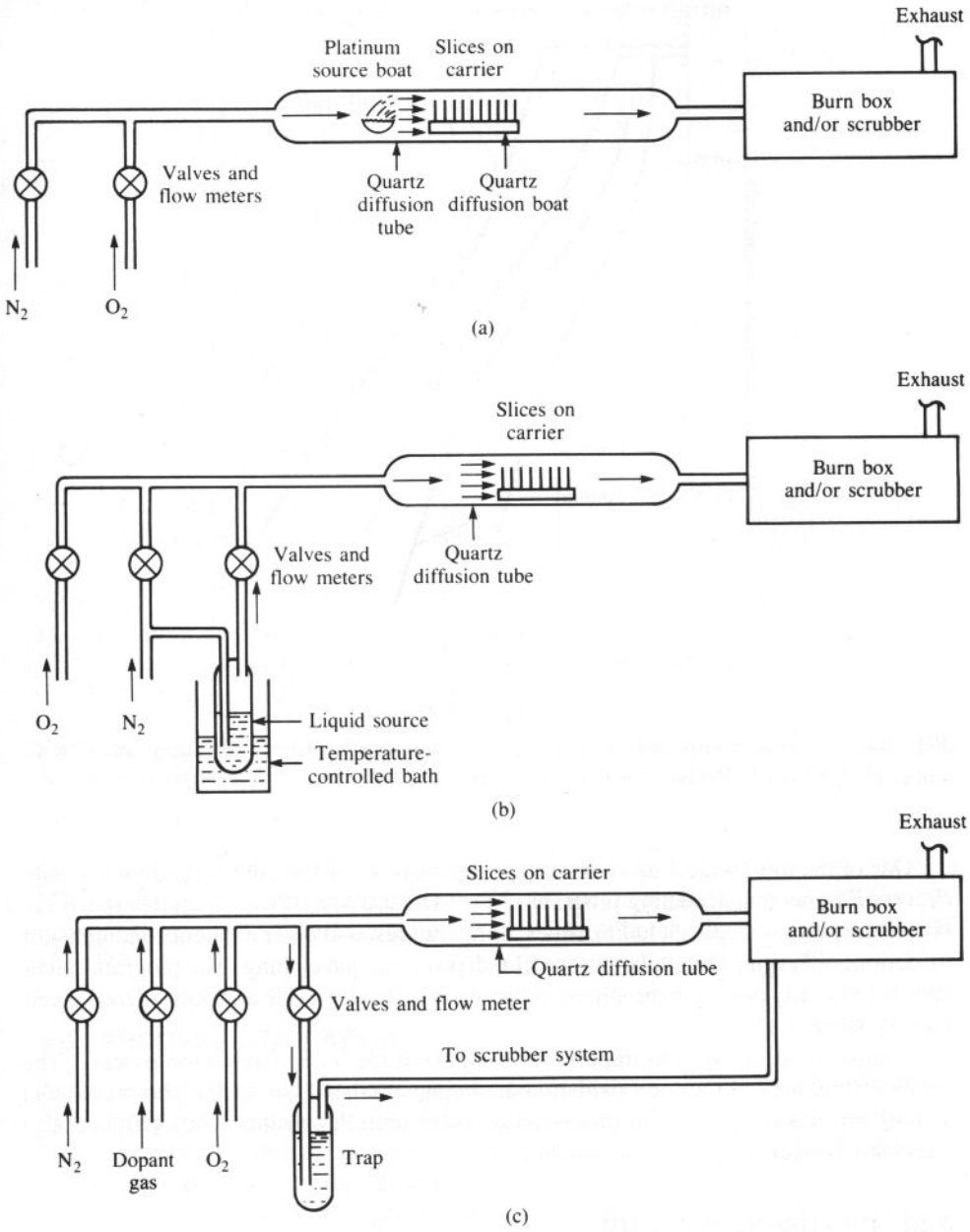


Fig. 4.22 Open-furnace-tube diffusion systems. (a) Solid source in a platinum source boat in the rear of diffusion tube; (b) liquid-source system with carrier gas passing through a bubbler; (c) diffusion system using gaseous impurity sources. Copyright John Wiley and Sons. Reprinted with permission from Ref. [23].

- **Ion Implantation:**
  1. Ion implanter is a high-voltage particle accelerator producing a high-velocity beam of impurity ions which can penetrate the surface of silicon target wafers. It contains **Ion Source** (produce plasma at high voltage 25kV)**, Mass Spectrometer** (bend ion beam to select desired impurity ion)**, High-Voltage Accelerator** (accelerate the beam up to 175 keV)**, Scanning System** (provide uniform implantation)**, and Target Chamber** (vacuum environment, hold wafers)**.**

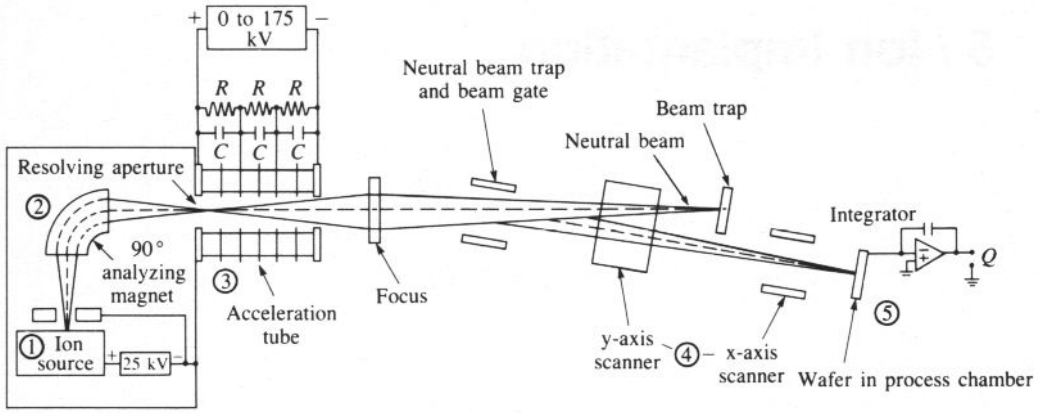


Fig. 5.1 Schematic drawing of a typical ion implanter showing (1) ion source, (2) mass spectrometer, (3) high-voltage accelerator column, (4) *x*- and *y*-axis deflection system, and (5) target chamber.

2. Mathematical Model

Gaussian distribution of concentration:

$$N(x) = N_p \exp^{-(x-R_p)^2/2\Delta R_p^2}$$

N_p: peak concentration.
R_p: Projected range
ΔR_p: Straggle (standard deviation)

Total dose:

$$Q = \int_0^\infty N(x)dx = \sqrt{2\pi} N_p \Delta R_p$$

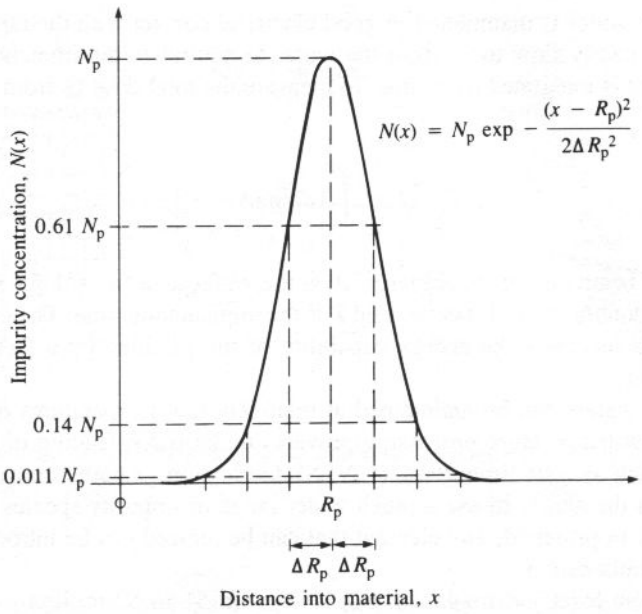


Fig. 5.2 Gaussian distribution resulting from ion implantation. The impurity is shown implanted completely below the wafer surface ($x = 0$).

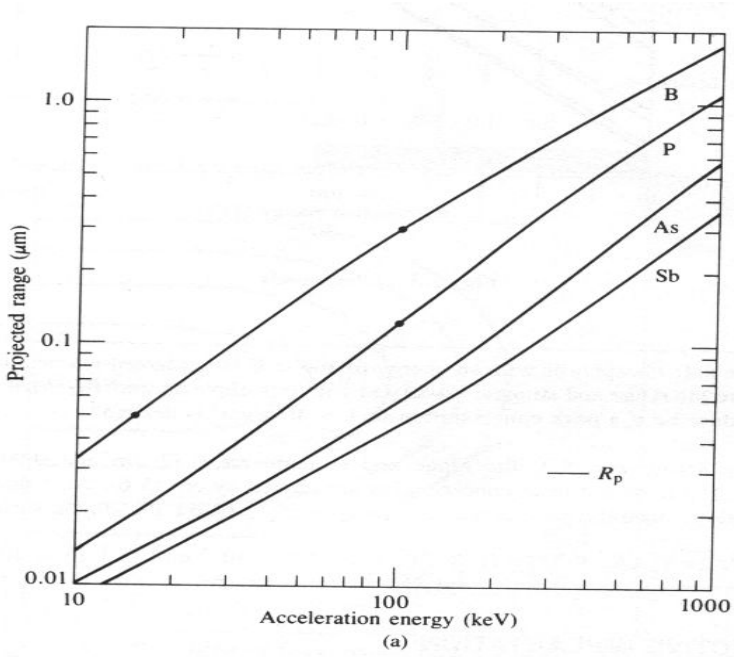


Fig. 5.3 Projected range and straggle calculations based on LSS theory. (a) Projected range R_p for boron, phosphorus, arsenic, and antimony in amorphous silicon. Results for SiO_2 and for silicon are virtually identical. (b) (On page 94) Vertical ΔR_p and transverse $\Delta R_\perp$ straggle for boron, phosphorus, arsenic, and antimony. Reprinted with permission from ref. [2]. (Copyright Van Nostrand Reinhold Company, Inc.)

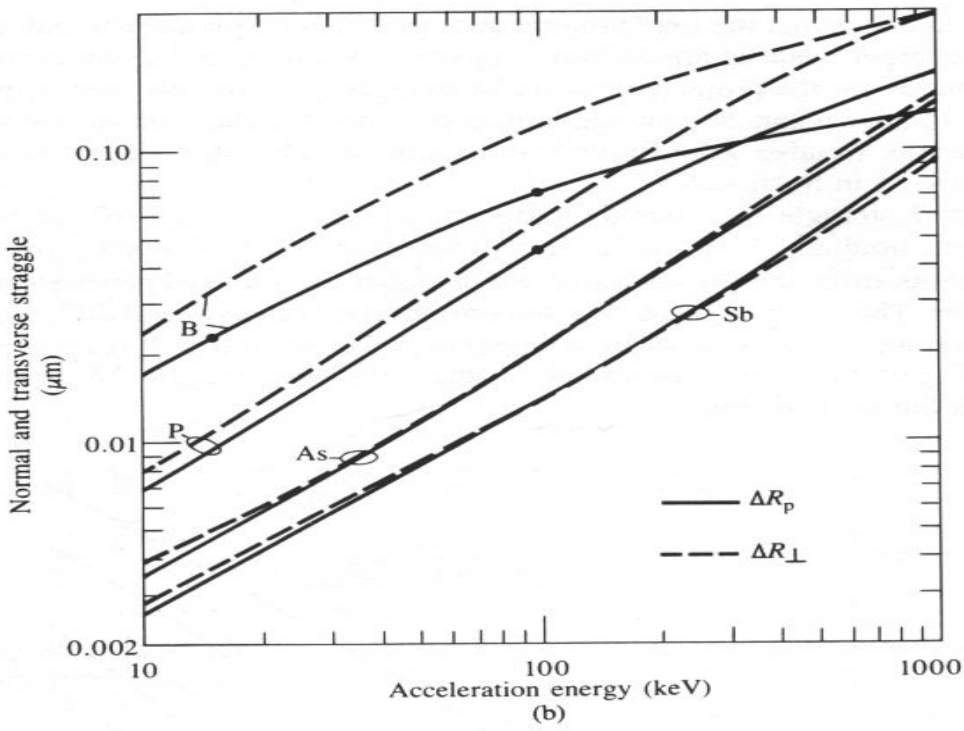


Fig. 5.3 (continued)

3. Selective Implantation

Use silicon dioxide or PR as mask.

- **Film Deposition**

1. Physical vapor deposition (PVD):

1-1. Evaporation: Filament and Electron-Beam Evaporation

Rate:

$$G = \frac{m}{\pi \rho r^2} \cos\phi \cos\theta \qquad \text{cm/sec}$$

for planetary holder, G is independent of substrate position:

$$G = \frac{m}{4\pi\rho r_0^{\,2}}$$ **for** $\cos\theta=\cos\Phi=r/2r_0$

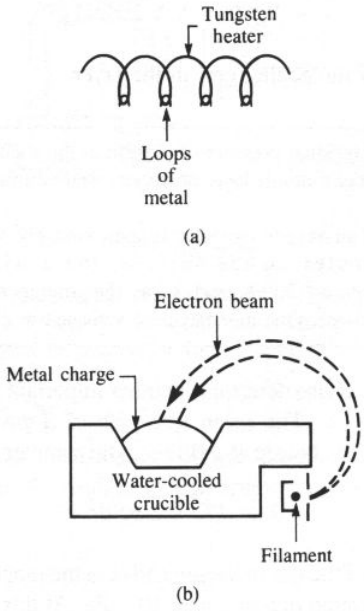


Fig. 6.2 Two forms of evaporation sources. (a) Filament evaporation, in which loops of wire hang from a heated filament; (b) electron-beam source in which a beam of electrons is focused on a metal charge. The beam is bent in a magnetic field.

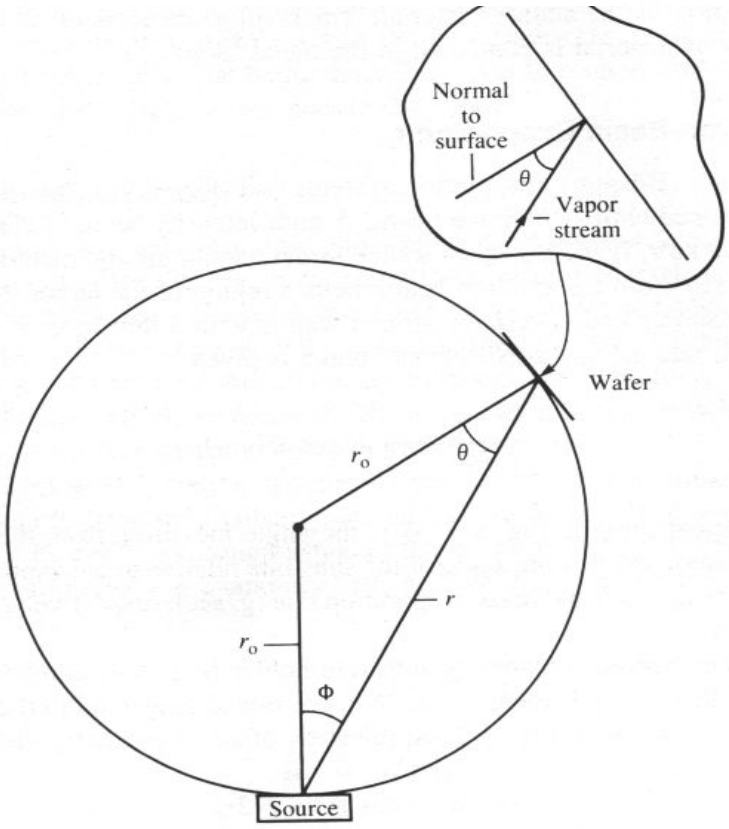
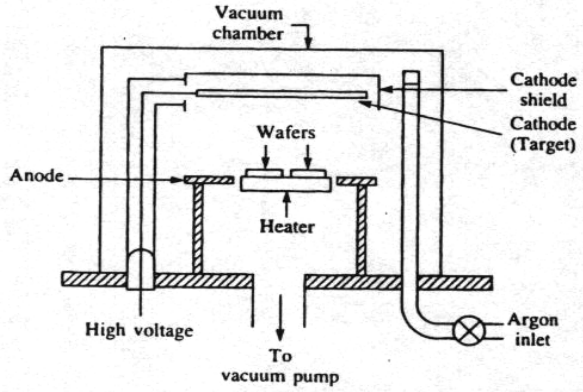
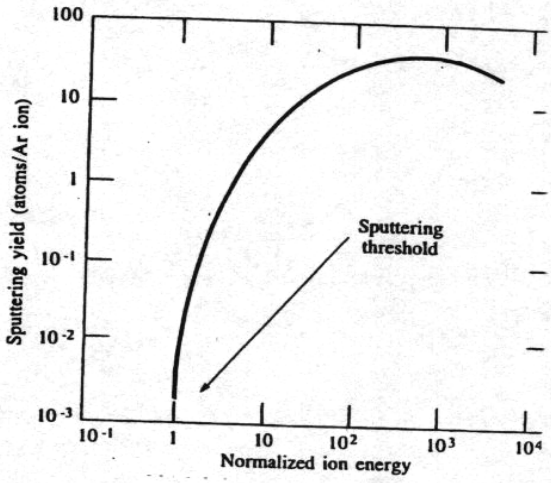


Fig. 6.3 Geometry for evaporation in a system using a planetary substrate holder.

1-2. Sputtering and sputtering etching





A dc sputtering system in which the target material acts as the cathode of a diode and the wafers are mounted on the system anode.

1-3. Shadowing and step coverage:

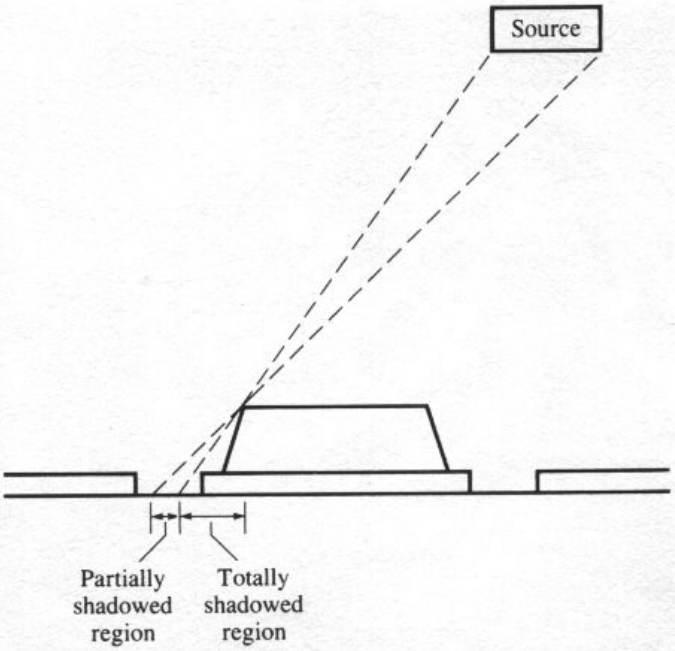


Fig. 6.5 An example of the shadowing problem that can occur in low-pressure vacuum deposition in which the molecular mean free path is large.

2. Chemical vapor deposition (CVD):

APCVD (Atmospheric-pressure): high gas flow rate, large wafers, continuously through, for passivation oxide

LPCVD (Low Pressure): hot wall, 300-1150 C, low pressure (30-250 Pa), SiO_2, Si_3N_4, Poly-Si, excellent uniformity, hundreds of wafers, but coat wall inside as well

PECVD (Plasma Enhanced): low temperature (200-400 C), RF generates plasma.

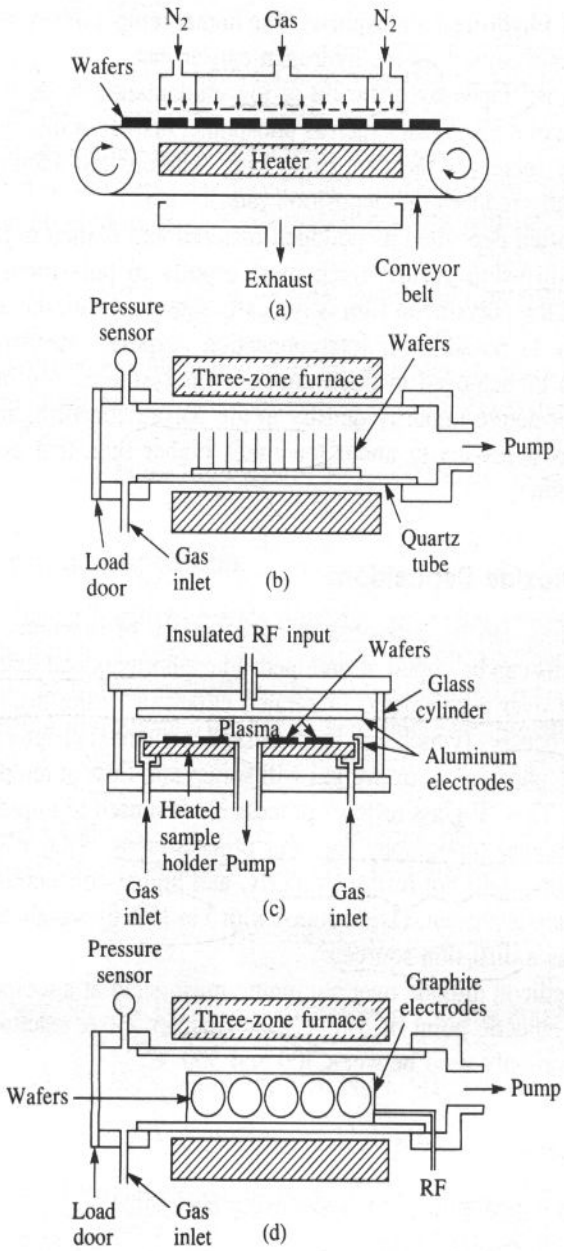


Fig. 6.8 Four types of chemical vapor deposition (CVD) systems. (a) Atmospheric-pressure reactor; (b) hot-wall LPCVD system using a three-zone furnace tube; (c) parallel-plate plasma-enhanced CVD system; (d) PECVD system using a three-zone furnace tube. Copyright, 1983, Bell Telephone Laboratories, Inc. Reprinted by permission from ref. [2].

2-1. Polysilicon Deposition (LPCVD, PECVD):

$$SiH_4 \xrightarrow{600^\circ C} Si + 2H_2$$

at 25-150 Pa, 600-650 C, 100-200 Å/min, can be doped during deposition

2-2. Silicon Dioxide Deposition (APCVD, LPCVD, PECVD):

$$SiH_4 + O_2 \longrightarrow SiO_2 + 2H_2$$

at300-500 C (less than 577 C for preventing silicon-aluminum eutectic reaction), can be doped with phosphorus, which re-flows at 1000-1100 C for improving step coverage.

Properties of Various Deposited Oxides.

Source	Deposition Temperature (°C)	Composition	Conformal Step Coverage	Dielectric Strength (MV/cm)	Etch Rate (Å/min) [100:1 H_2O:HF]
Silane	450	$SiO_2(H)$	No	8	60
Dichlorosilane	900	$SiO_2(Cl)$	Yes	10	30
TEOS	700	SiO_2	Yes	10	30
Plasma	200	$SiO_{1.9}(H)$	No	5	400

2-3. Silicon Nitride Deposition (LPCVD, PECVD):

LPCVD

$$3SiH_4 + 4NH_3 \xrightarrow{700-900^\circ C} Si_3N_4 + 12H_2$$

or

$$3SiCl_2H_2 + 4NH_3 \xrightarrow{700-800^\circ C} Si_3N_4 + 6HCl + 12H_2$$

PECVD

$$SiH_4 + NH_3 \xrightarrow{300-450^\circ C} SiNH + 3H_2$$

2-4. CVD Metal deposition:
Mo, Ta, Ti, W.

- **Interconnections and contacts:**
  Requirements: Low sheet resistance, Low capacitance, and Low contact resistance. Al is widely used for metal interconnections in IC process.

1. Metal interconnection

⇨ **Low resistivity: Al 2.7 μ ohm-cm and adhere well to SiO_2**

⇨ **Ohmic contact:**

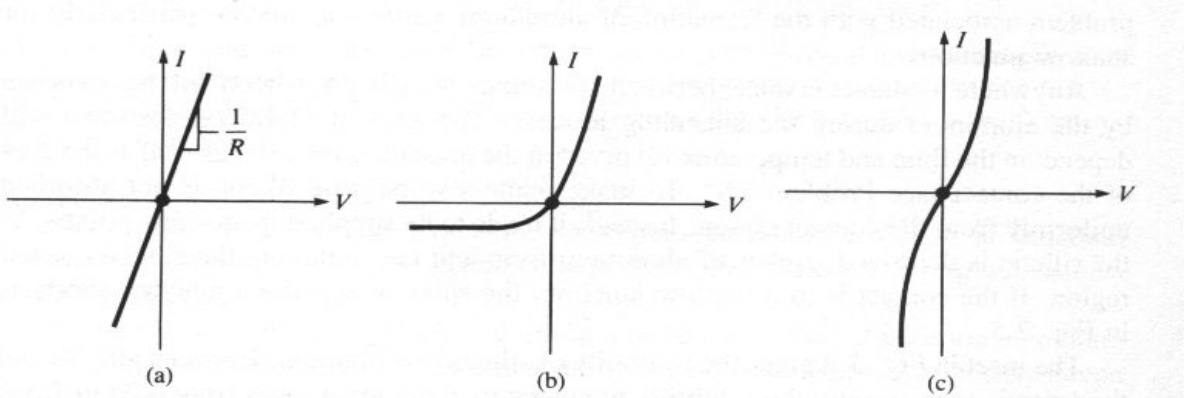


Fig. 7.2 *I-V* characteristics of contacts between integrated-circuit materials. (a) Ideal ohmic contact; (b) rectifying contact; (c) practical nonlinear "ohmic" contact.

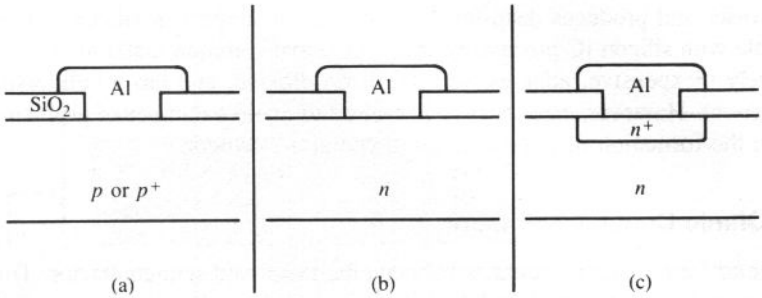


Fig. 7.3 Three possible types of aluminum contacts to silicon. (a) Aluminum to *p*-type silicon forms an ohmic contact with an *I-V* characteristic approximating that in Fig. 7.2a; (b) aluminum to *n*-type silicon can form a rectifying contact (Schottky barrier diode) like that in Fig. 7.2b; (c) aluminum to n^+ silicon yields a contact similar to that in Fig. 7.2c.

2. Diffused interconnections

- ⇨ **Minimum resistivity ~ 1000 μ ohm-cm, yielding a typical sheet resistance 10-20 ohms/□ (for shallow structure about 1 μm deep).**
- ⇨ **High capacitance between the diffused layers and substrate.**

3. Polysilicon interconnections

- ⇨ **Heavily doped n-type polysilicon is used as the MOS gate material.**
- ⇨ **Heavily doped polysilicon yields a minimum resistivity of 300 μ ohm-cm (20-30 ohms/□ for shallow diffused interconnections), which is not low enough for long distance connection.**
- ⇨ **Substantial capacitance**

4. Silicides, polycides, and Salicides

- ⇨ **Silicides: Noble or refractory metals reacting with silicon to form silicides (compounds), which provide low-resistivity (typically 15-50 μ ohm-cm) contact to silicon. for example: $TiSi_2$, WSi_2, $CoSi_2$, etc…**
- ⇨ **Polysides: on polysilicon**
- ⇨ **Salicides: self aligned silicides.**