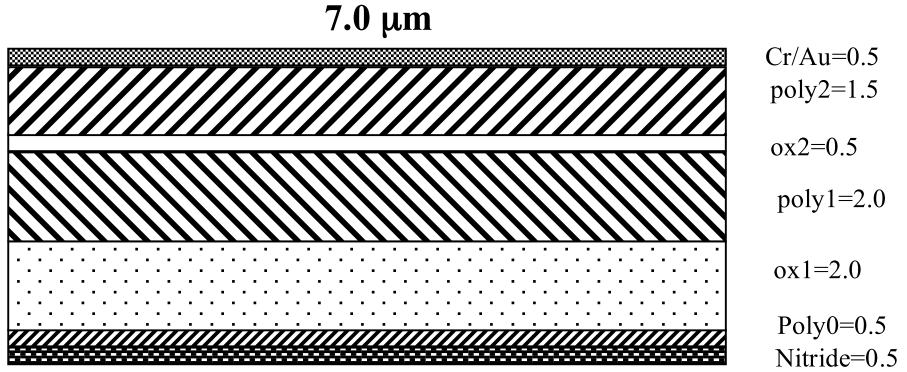
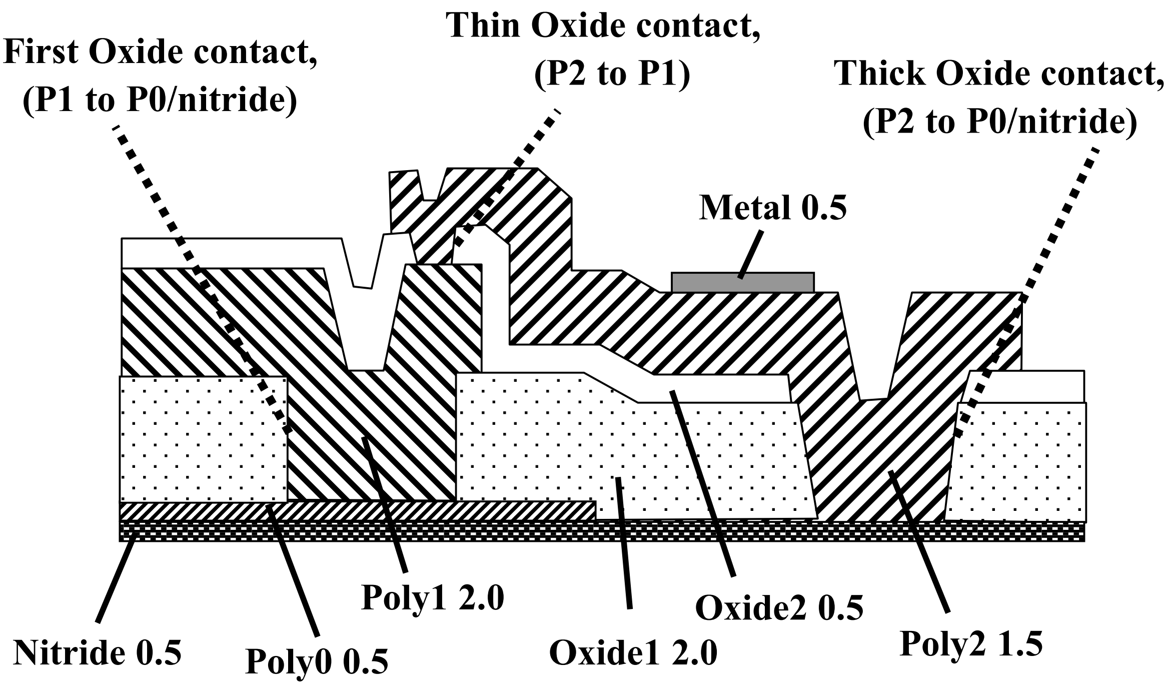
Lecture 8-1 MCNC/MUMPS Process

◆ **MCNC/MUMPS structure**

Layers provided:



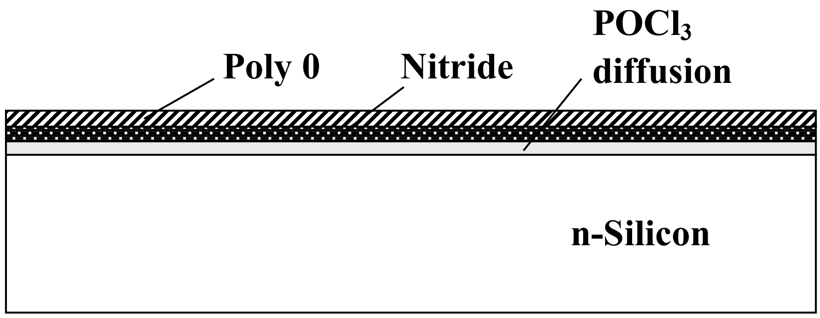
MUMPS Cross section with possible contacts:



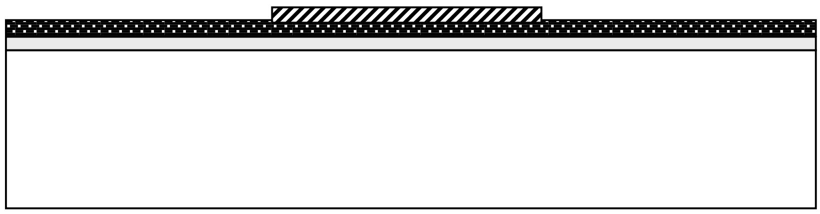
Notice: 1. Substrate used: 100mm n-type (100) silicon wafers of 0.5 Ω-cm resistivity.

2. Substrate surface are heavily doped with phosphorus to reduce charge feed through to the substrate from electrostatic devices on the surface.

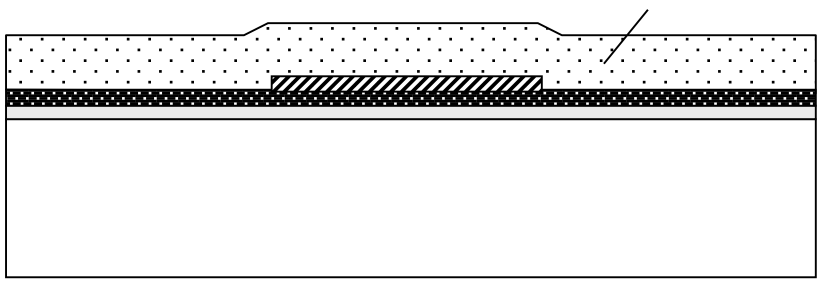
◆ Detail Fabrication process of MCNC/MUMPS



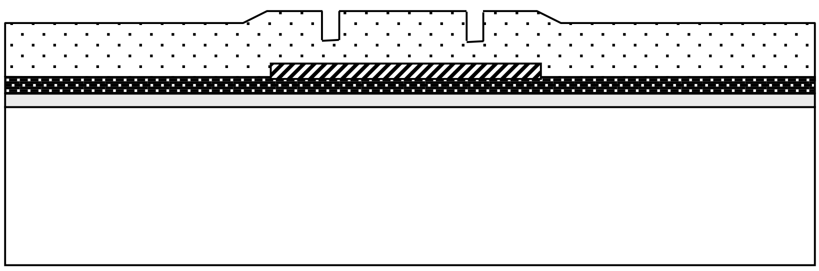
1. Heavy phosphorus doping
2. 0.5 µm silicon nitride Deposition
3. 0.5 µm low stress polysilicon deposition and annealing



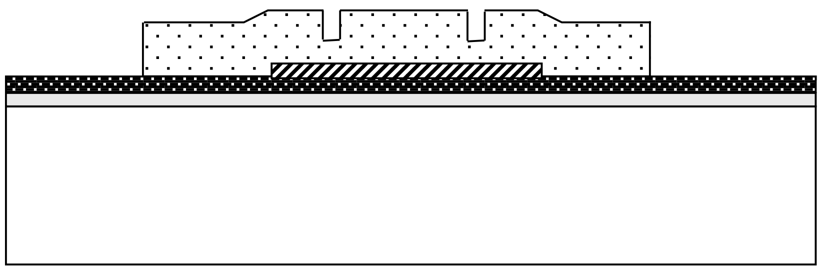
4. RIE patterns Poly0 (#1 POLY0)



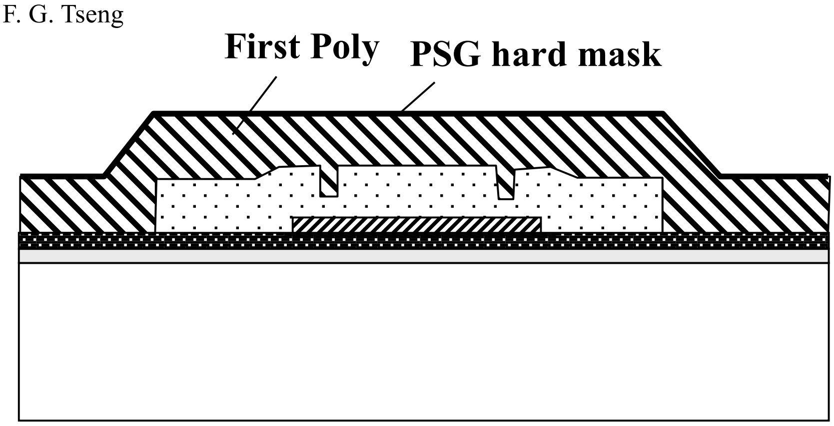
5. 2.0 µm first PSG deposition



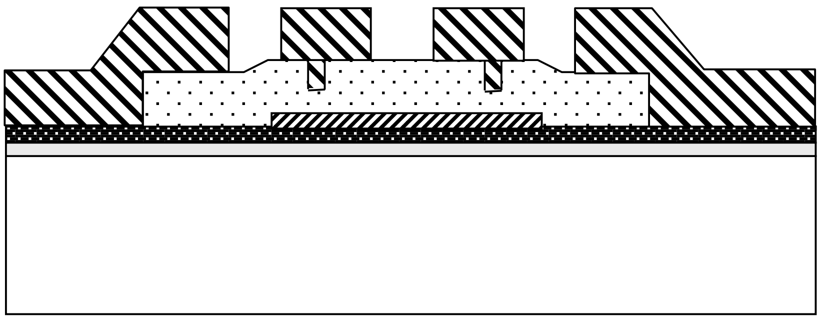
6. RIE pattern 0.75 µm dimple (#2 DIMPLE)



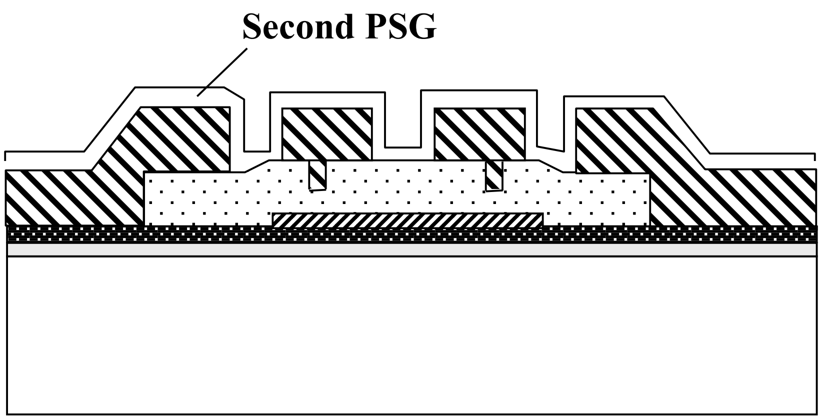
7. RIE pattern 2 µm contact hole to poly0/nitride (#3 FIRST OXIDE)



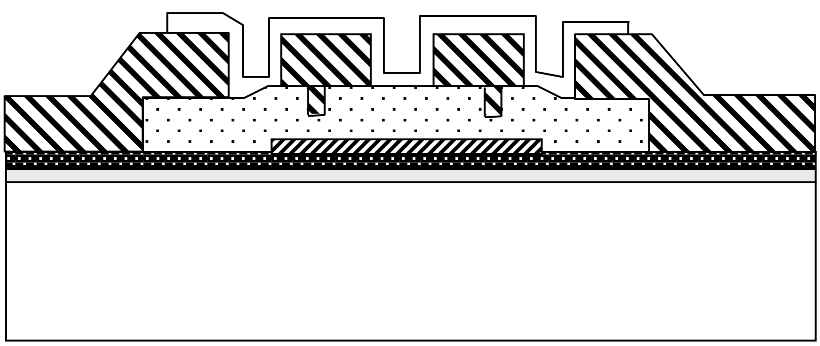
8. 2 μm polysilicon deposition
9. 0.2 μm PSG deposition
10. Annealed at 1050 °C



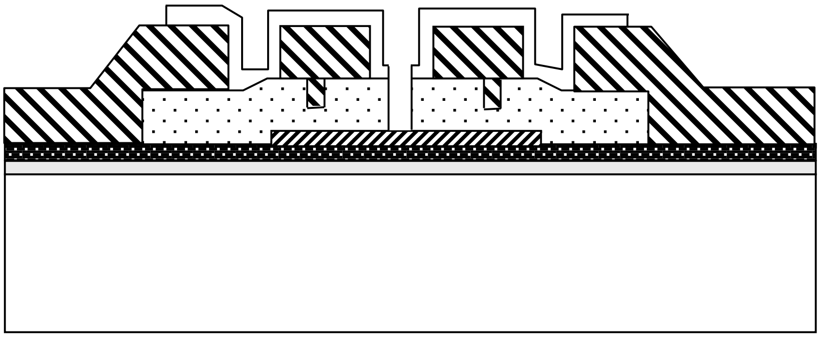
11. RIE etch PSG hard mask
12. RIE pattern first polysilicon (#4 FIRST POLY)



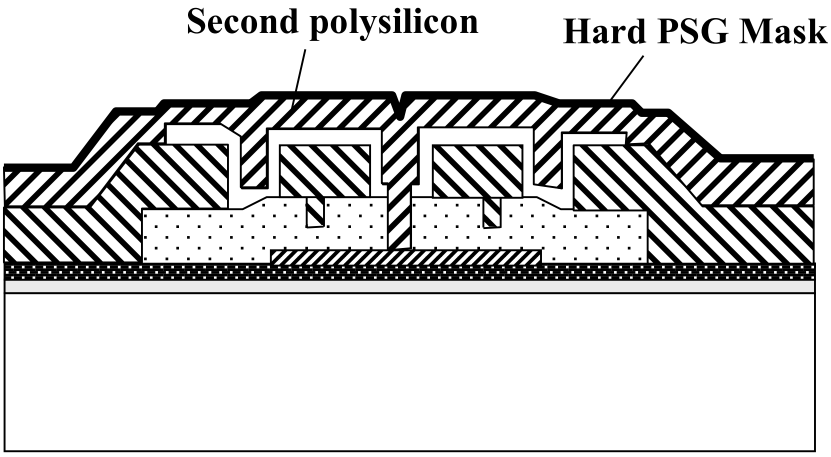
13. Second PSG (0.5 μm) deposition



13. RIE pattern contact hole to poly1 (#5 THIN)

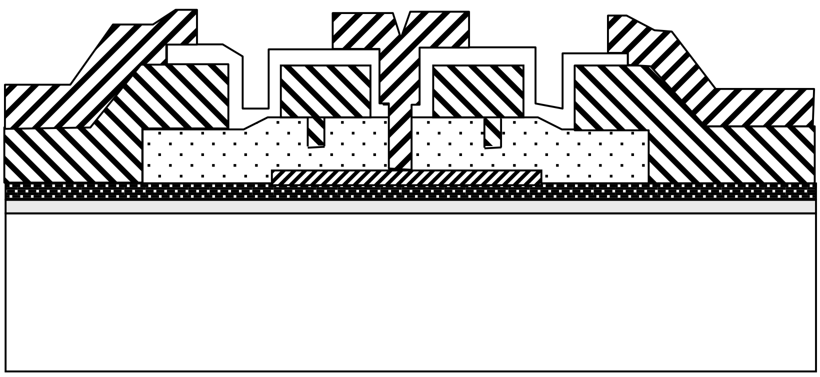


14. RIE pattern contact hole to poly0/nitride (#6 THICK)



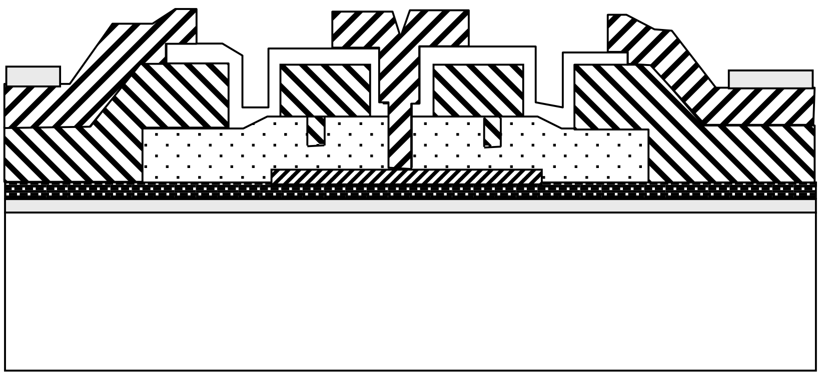
15. 1.5 μm polysilicon deposition

16. 0.2 μm PSG deposition



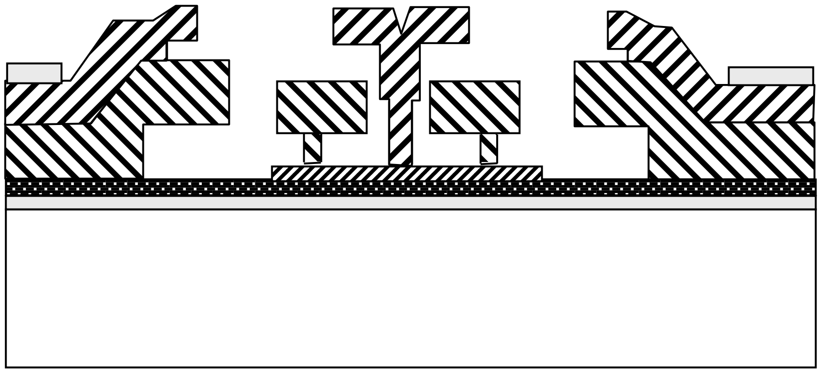
17. RIE etch PSG hard mask

18. RIE pattern second polysilicon (#7 SECOND POLY)



19. 0.5 μm Metal deposition

20. Lift metal (#8 METAL)



21. Concentrate HF 2.5 min to release structure

◆ MCNC/MUMPS process layer names:

Layer	Dep/Diff	Contact	Cif name	GDS II #	Color (L.)
Poly Zero	Poly		CPZ	13	Orange fill
First Oxide		P1/p0	COF	43	Grey cross
Dimple			COS	50	Black box
First Poly	Poly		CPS	45	Red fill
Thin Oxide		P2/p1	COT	47	Thin line
Thick oxide		P2/p0	COL	52	Thick line
Second Poly	Poly		CPT	49	Grey fill
Metal	Metal		CCM	51	Blue fill
Hole 1		P1 release hole	CHO	0	Red box
Hole 2		P2 release hole	CHT	1	Grey box

Typical sheet resistance for poly0~ 20, poly1~ 10, poly2~ 14, and metal~ 0.05 Ω/□

◆ Design rules:

EZ design rules:

Line and space size ≥ 3 μm

Overlap and border ≥ 5 μm

Distance between releasing holes ≤ 30 μm

Detail design rules:

Check Cornos/MUMPS process introduction and design rules, or web:
http://www.memsrus.com/cronos/svcsmumps.html

◆ Process and Design Issues:

1. **To remove large region of thick Poly while oxide hole not cover of polysilicon—pose nitride/poly0 etch away and poly short to the substrate.**

2. **Use FIRST OXIDE+THIN to replace THICK—misalignment problem causes underneath poly0 and nitride etch away**

3. **Improper pad design: FIRST OXIDE cut larger than poly1 pad area-- pose nitride/poly0 etch away during the poly 2 etching and poly may short to the substrate.**

4. **Thick Oxide cut without poly2 cover-- pose nitride/poly0 etch away during the poly 2 etching and poly may short to the substrate.**

5. **Metal (here is Cr/Au) is not easy to be survive in HF release etching. Try to shorten the release time by put frequent etch holes or not to use metal. Metal is always on the top of poly2 without dielectric material between. Care need to be taken if**

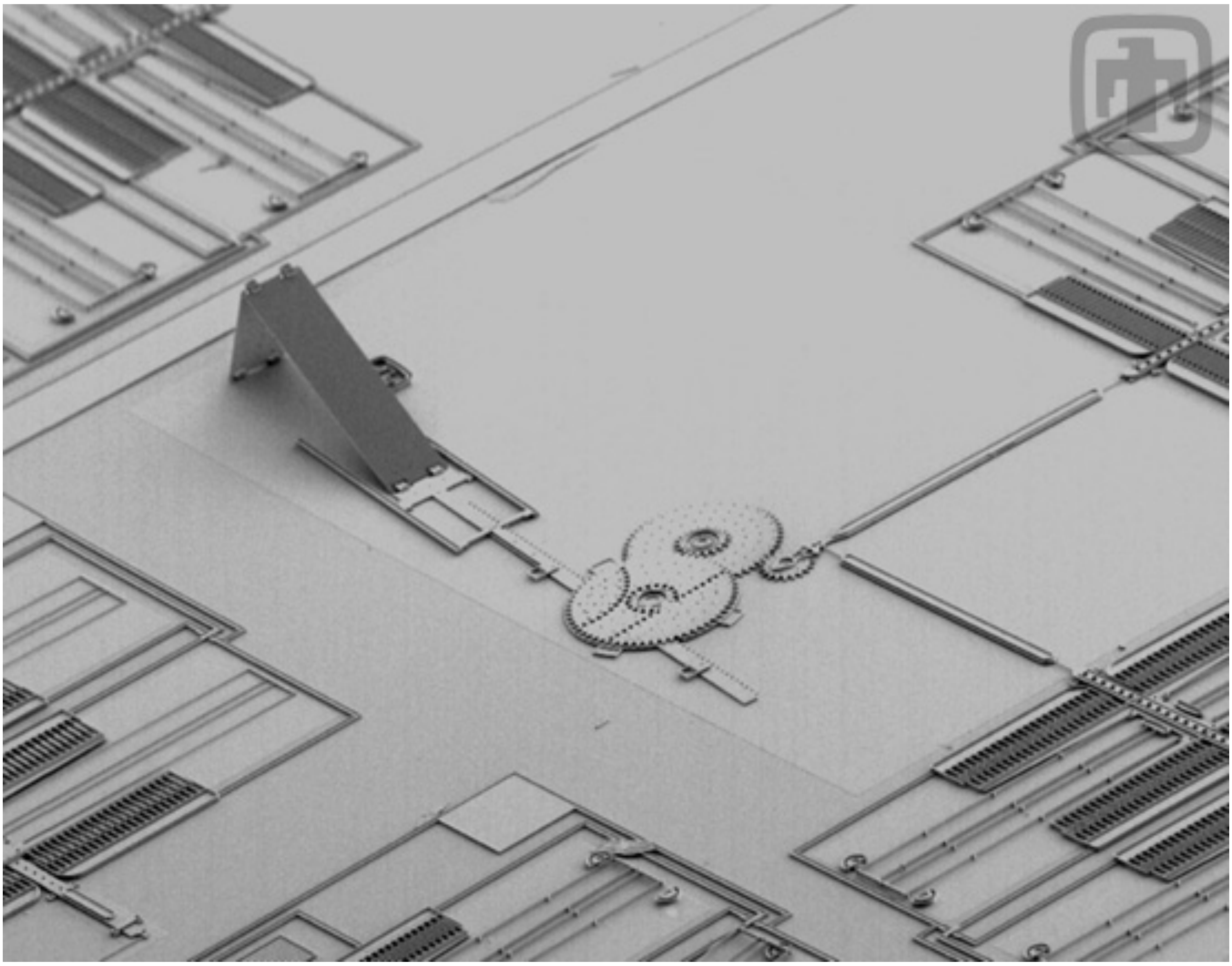
the metal needs to be placed on top on poly1 or poly0.

◆ **Possible Structures made by MCNC/MUMPS**

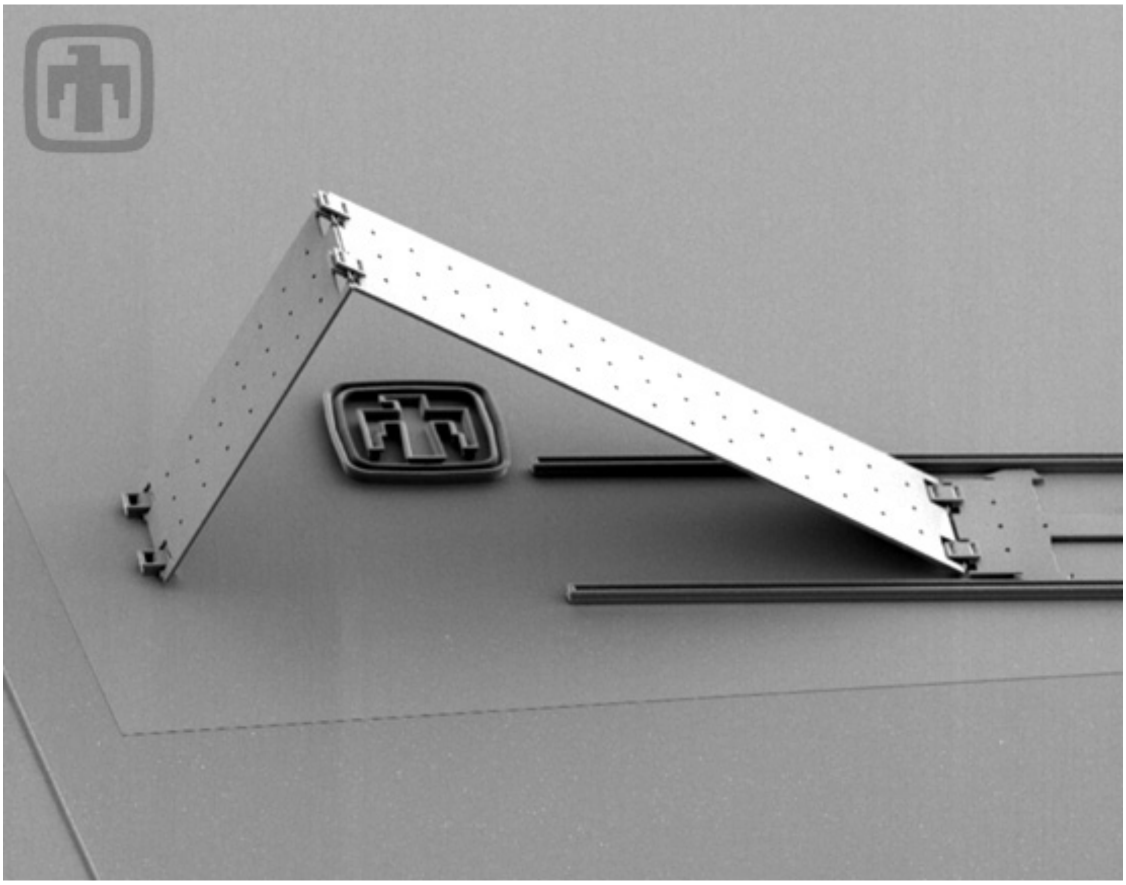
Pictures adopted from:

http://www.mdl.sandia.gov/micromachine

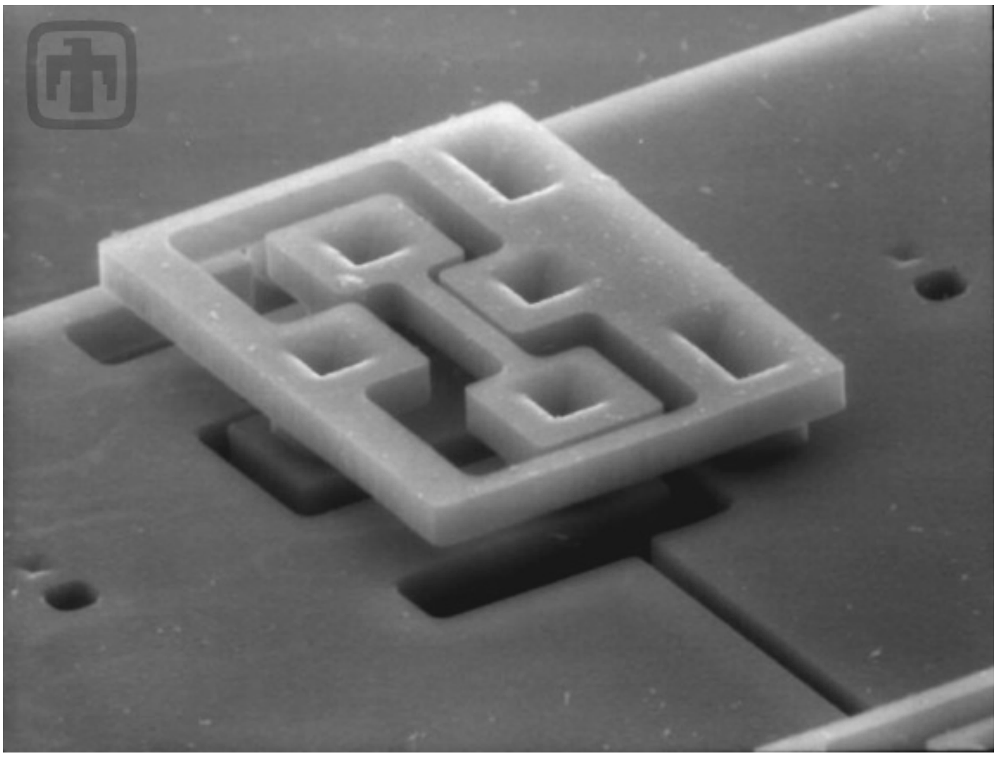
Micro Mirror System



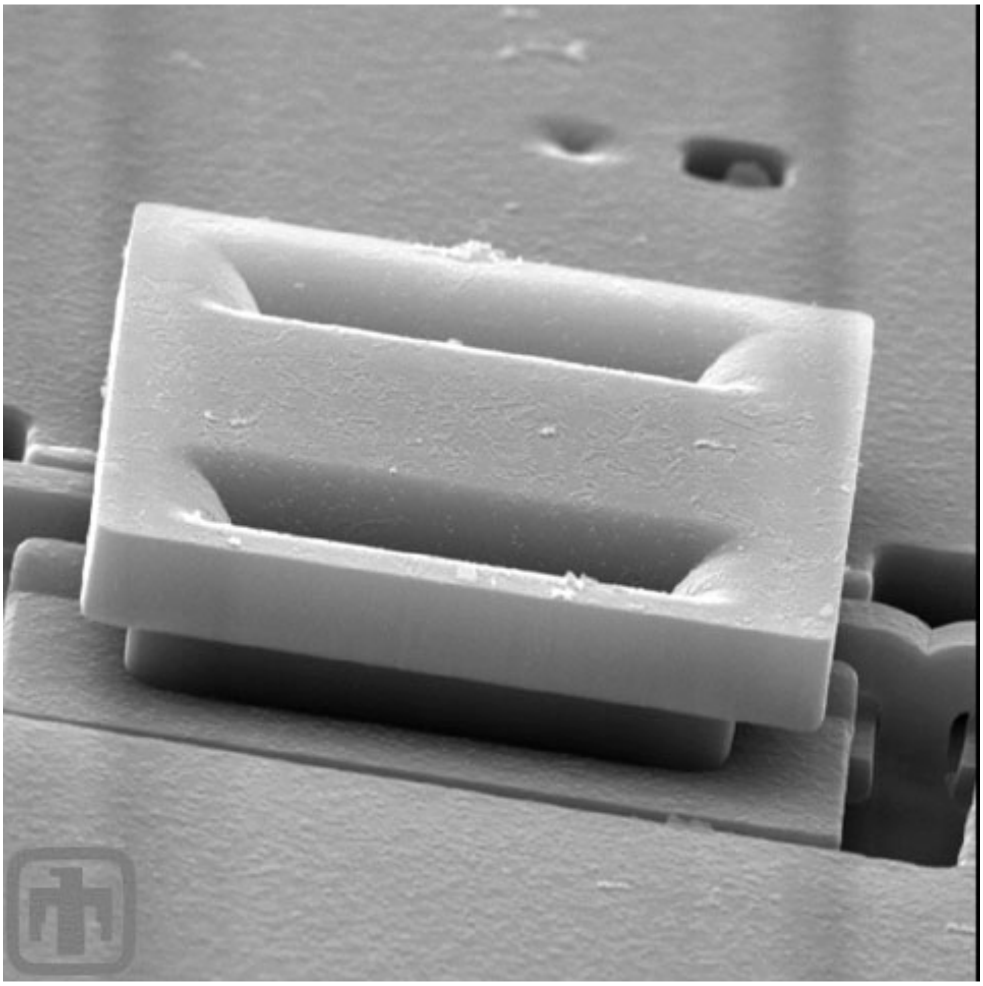
Micro Mirror:



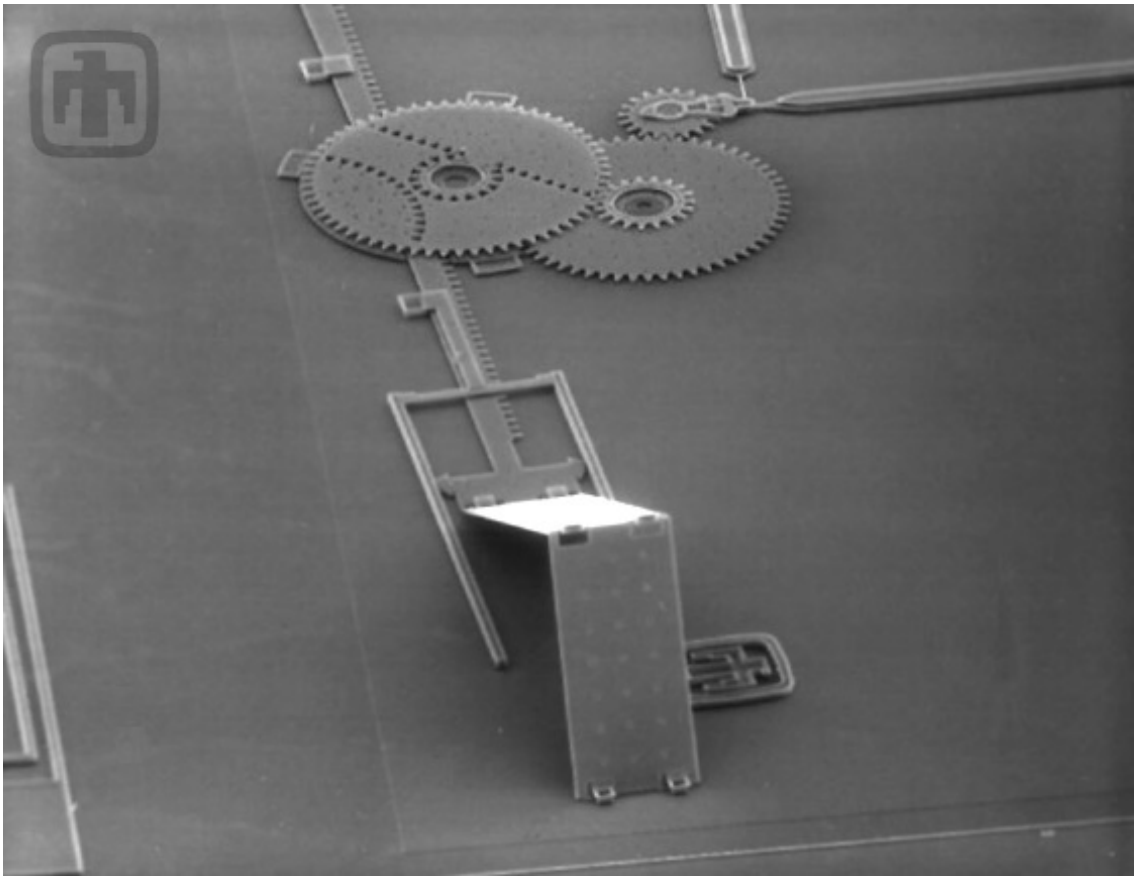
Hinge 1:



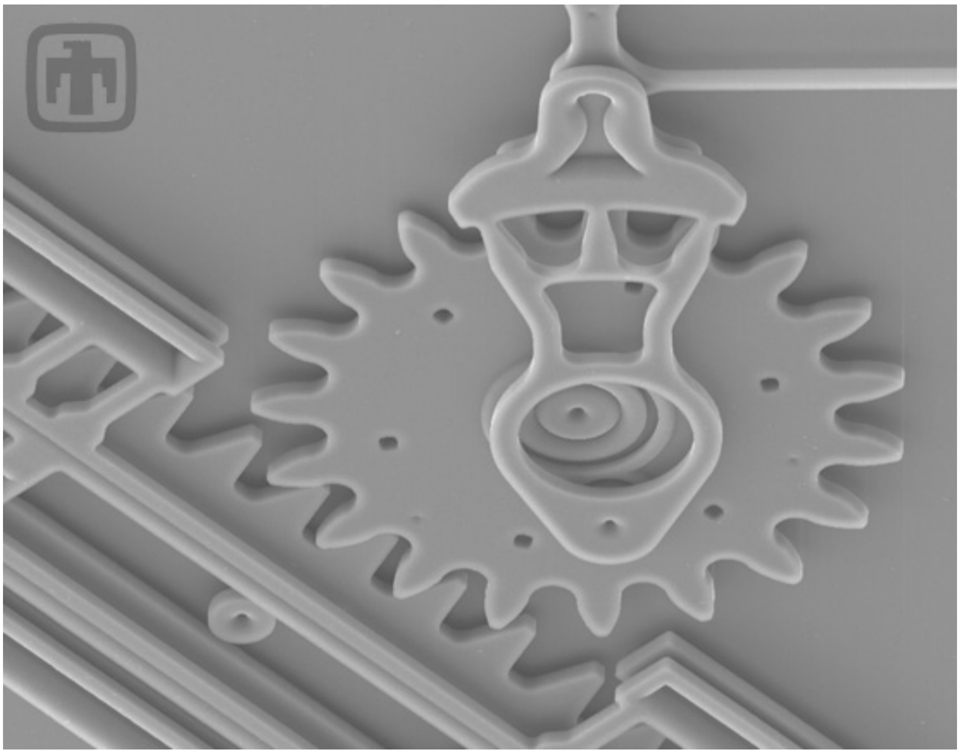
Hinge 2:



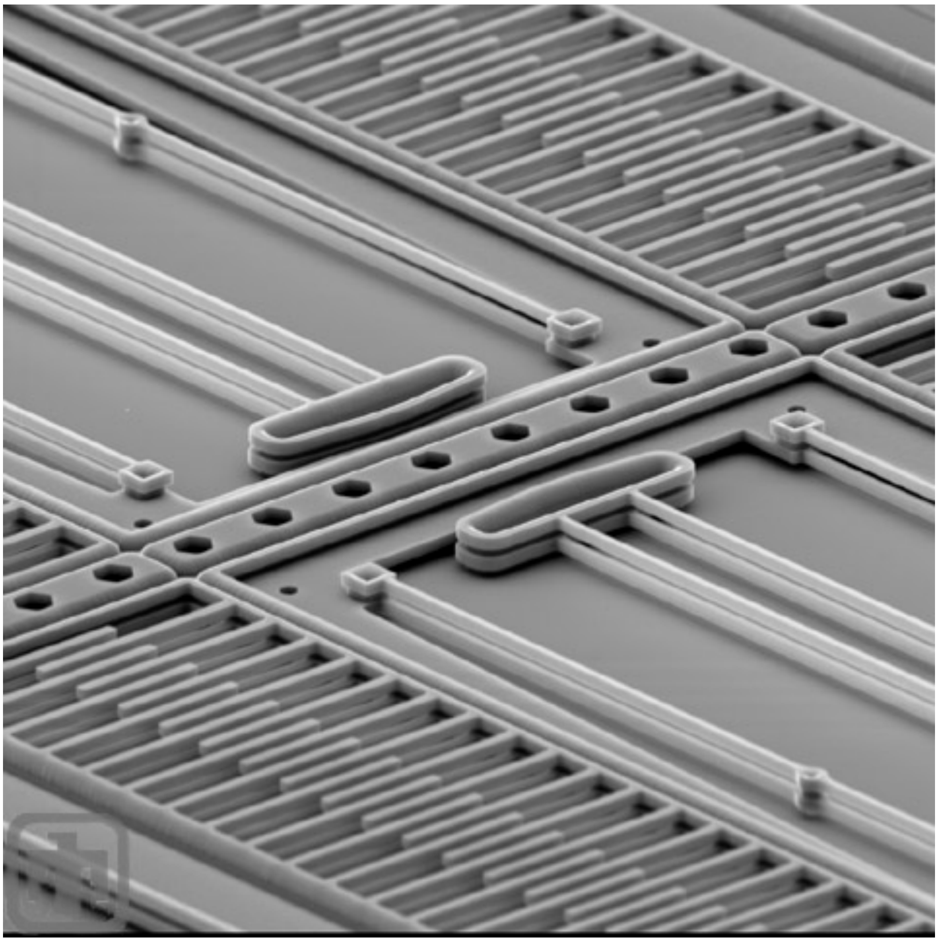
Driving gear set:



Driving gears:



Linear comb drive:



Srping joint: